ANALYSIS OF GRID SYNCHRONIZATION TECHNIQUES FOR DISTRIBUTED GENERATION SYSTEM DURING GRID ABNORMALITIES

A THESIS SUBMITTED IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF

Master of Technology

In

Power Control and Drives

By

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National Institute of Technology, Rourkela
Rourkela-769008

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ODISHA, INDIA

CERTIFICATE

This is to certify that the Thesis entitled "ANALYSIS OF GRID SYNCHRONIZATION TECHNIQUES FOR DISTRIBUTED GENERATION SYSTEM DURING GRID ABNORMALITIES", submitted by Mr. CH H S RAVI TEJA bearing roll no. 211EE2330 in partial fulfillment of the requirements for the award of Master of Technology in Electrical Engineering with specialization in "Power Control and Drives" during session 2011-2013 at National Institute of Technology, Rourkela is an authentic work carried out by him under our supervision and guidance.

To the best of our knowledge, the matter embodied in the thesis has not been submitted to any other university/institute for the award of any Degree or Diploma.

Date: 03/06/2013 Supervisor

Place: Rourkela Prof. B. Chitti Babu

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M.Tech PCD 4th Sem

ABSTRACT

This thesis presents a synchronization algorithm aimed to provide an estimation of the angular frequency, and both the positive and negative sequences of the fundamental component of an unbalanced and distorted three-phase reference signal. It does not require transformation of variables into the synchronous frame coordinates as other conventional phase-locked loop (PLL) schemes. Thus it is not based on the phase angle detection. Instead the angular frequency is detected and used for synchronization purposes. The design of UH-PLL, is based on a complete description of a three-phase signal which involves both positive and negative sequences in stationary coordinates of the fundamental and harmonic components. Also it includes an explicit harmonic compensation mechanism to alleviate the effect of harmonic distortion and unbalances in the supply. Therefore UH-PLL is intended to perform properly under severe unbalanced conditions, subject to distortion caused by low harmonics, and is insensitive against angular frequency variations, and sags and swells in the three-phase reference signal.

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CHAPTER 1

Introduction

1.1 MOTIVATION:

The Environmental friendly renewable energy technologies such as wind and solar energy systems are among the fleet of new generating technologies driving the demand for distributed generation of electricity. Power Electronics has initiated the next technological revolution and enables the connection of distributed generation (DG) systems to the grid. Thus the increasing power demand will be met by Distributed Generation (DG) system which are based on renewable energy sources such as solar power, wind power, small hydro power etc. [1]-[2]. These systems need to be controlled properly in order to ensure sinusoidal current injection into grid. However, they have a poor controllability due to their intermittent characteristics [3]. Grid connected inverter plays a vital role in maintaining voltage at the point of common coupling (PCC) constant. For the reliable operation of utility grid based on DG system, the power plant operators should satisfy the grid code requirements such as fault ride through, grid stability, grid synchronization and power control etc. The major issue associated with DG system is their synchronization with utility voltage vector [4]. The information about the phase angle of utility voltage is tracked accurately to control the flow of active and reactive power and to turn on and off power devices.

1.2 LITERATURE REVIEW:

Due to the increased number of DPGS connected to utility grid, instability of the DG systems and of the grid itself are subjected to instability problems. One of the important issues of the DPGS connected to the utility network is the synchronization with the grid voltage vector [6].The detection of the positive sequence voltage component at fundamental frequency is required for the control of distributed generation. The magnitude and phase angle of the positive sequence voltage is used for the synchronization of the converter output variables or for the transformation of the state variables into rotating reference. Regardless of the technique used in the system detection i.e. using a Zero Crossing Detector (ZCD) or a Phase Locked Loop (PLL), the amplitude and the phase angle of the positive sequence component must be fast and accurately obtained, even if the utility voltage is distorted or unbalanced[5]. Among these techniques the voltage zero-crossing is the simplest one and the phase-locked loop (PLL)-based techniques are the state-of-the-art techniques in detecting the phase angle of the grid voltages [1], [6]-[12].

THESIS OBJECTIVES:

The following objectives have been achieved at the end of the project.

1) To analyze various grid synchronization Techniques available for phase angle tracking.

2) To study the conventional SRF Phase Locked Loops (PLL) and observe its response during grid unbalances.

3) To study the advanced PLL techniques (DSRF PLL and UH-PLL) and their response during abnormal grid conditions such as line to ground fault and various power quality problems. The power quality problems constitute of voltage unbalances, voltage sag, voltage dip, harmonic injection etc.

4) To study the response of the UH-PLL in order to analyze the stability of the system.

5) To observe the differences between DSRF PLL and UH-PLL to detect the phase angle and the angular frequency respectively during various abnormal grid conditions and power quality problems.

1.3 Organization of thesis:

The thesis is organized into five chapters including the introduction in the Chapter 1. Each of these is summarized below.

Chapter 2: Deals with the introduction of various grid synchronization algorithms used for power converters. A brief idea is given about various grid code requirements that need to be satisfied for proper operation of the DG system. It is followed by the analysis of various grid synchronization algorithms including Zero Crossing Detector (ZCD), Synchronous Reference Frame (SRF) PLL, Double Synchronous Reference Frame (DSRF) PLL and UH-PLL.

Chapter 3: Describes the analysis and response of DSRF PLL. Initially an idea of SRF PLL, its mathematical modelling, working and response during unbalanced grid condition are shown and shows how it fails to track the phase angle for unbalanced condition accurately. This is followed by the detailed mathematical analysis of DSRF PLL to show how it decouples the positive and negative sequence components and track the phase angle even under abnormal grid conditions. Finally, the simulation results showing the response of DSRF PLL under various abnormal grid conditions as obtained by simulations in MATLAB/SIMULINK.

Chapter 4: Describes the analysis and response of UH-PLL. It starts with a brief introduction about the UH-PLL, its mathematical analysis and working. This is followed by the response of UH-PLL during abnormal grid conditions and illustrates how it tracks the angular frequency and phase angle of the positive and negative sequence components.

Chapter 5: Reveals the general conclusions of the work done and the references.

CHAPTER 2

Grid Synchronization Techniques for Power Converters

2.1 Introduction:

Converter interfaced DG units must be synchronized with the utility system. Grid synchronization is a challenging task especially when the utility signal is polluted with disturbances and harmonics or is of a distorted frequency. A phase detecting technique provides a reference phase signal synchronized with the grid voltage that is required to control and meet the power quality standards. This is critical in converter interfaced DG units where the synchronization scheme should provide a high degree of insensitivity to power system disturbances, unbalances, harmonics ,voltage sags, and other types of pollutions that exist in the grid signal [1], [6]. In general, a good synchronization scheme must i) proficiently detect the phase angle of the utility signal, ii) Track the phase and frequency variations smoothly, and iii) forcefully reject disturbances and harmonics. These factors, together with the implementation simplicity and the cost are all important when examining the credibility of a synchronization scheme.

2.2 GRID CODE REQUIREMENTS:

A grid code is a specification which defines the parameters a facility connected to an electric network has to meet to ensure safe, secure and proper economic functioning of the electric system. These include voltage regulation, reactive power supply and power factor limits, response to a system fault (short-circuit), response to changes in the frequency on the grid, and requirement to "ride through" short interruptions of the connection [7].

2.2.1 Voltage regulation: This means that by the connecting the DG, the voltage at the PCC shall not be outside a specified range.

2.2.2 Frequency Deviation:

In the same way the frequency deviations shall also not go outside a specified range.

2.2.3 Synchronization:

While synchronizing a DG with a utility grid it shall not cause a voltage fluctuation of more than ± 5% of the existing voltage level at the Point of Common Coupling (PCC).

2.2.4 Monitoring Systems:

A DG system of rating 250 kW or more shall have provisions for the monitoring of connection status and real and reactive power outputs at the point of DG connection.

2.2.5 Isolation system:

Whenever required by utility grid operating practice for making or breaking the connection, an isolation device shall be located between the DG unit and the utility grid.

2.2.6 Harmonics:

The allowable voltage harmonic distortion is specified at the PCC. It is normally required that the maximum voltage total harmonic distortion is 5% and maximum individual frequency voltage harmonic is 3% of the fundamental component.

2.2.7 DC current injection:

A DG and its interconnection system shall not inject dc current greater than 0.5% of its rated output current into the utility grid at the PCC.

2.2.8 Flicker:

A DG must not create objectionable flicker for customers on the Utility grid.

2.3 GRID SYNCHRONIZING TECHNIQUES:

2.3.1 Zero Crossing Detector (ZCD):

Zero-crossing detector is an applied form of a comparator. Either of the op-amp based circuits discussed can be employed as zero-crossing detector. In some applications the input signal may be low frequency one (i.e. input may be a slowly changing waveform). In such a case output voltage may not switch quickly from one saturation state to another. Because of the noise at the input terminals of op-amp, there may be fluctuation in output voltage between two saturation states (+ Vsat and – Vsat voltages) [7]. Thus zero crossing may be detected for noise voltages as well as input signal. Both problems can be overcome if we use regenerative or positive feeding causing the output voltage to change faster and eliminating the false output transitions that may be caused due to noise at the input of the op-amp. Thus we prefer PLL based methods for the detection of Phase angle when compared to Zero Crossing Detector [7].

2.3.2 Phase Locked Loop (PLL):

A phase-locked loop is a control system that generates an output signal whose phase is related to the phase of an input "reference" signal [5].This circuit compares the phase of the input signal with the phase of the signal derived from its output oscillator and adjusts the frequency of its oscillator to keep the phases matched. The output signal from the phase detector is used to control the oscillator in a feedback loop. Frequency is the time derivative of phase. Keeping both the input and output phase in lock step implies keeping the input and output frequencies in lock step. Consequently it can track an input frequency or it can generate a frequency that is a multiple of the input frequency.

A. Synchronous Reference Frame (SRF) PLL:

In the conventional PLL, three-phase voltage vector is translated from the abc natural reference frame to the αβ stationary reference frame by using Clarke's transformation, and then translated to dq rotating frame by Park's transformation as shown in Fig. 2.1 [5]. The angular position of this dq reference is controlled by a feedback loop which makes the q-axis component equal to zero in

steady state. Therefore, under steady state condition, the d-axis component will be the voltage vector amplitude [5].

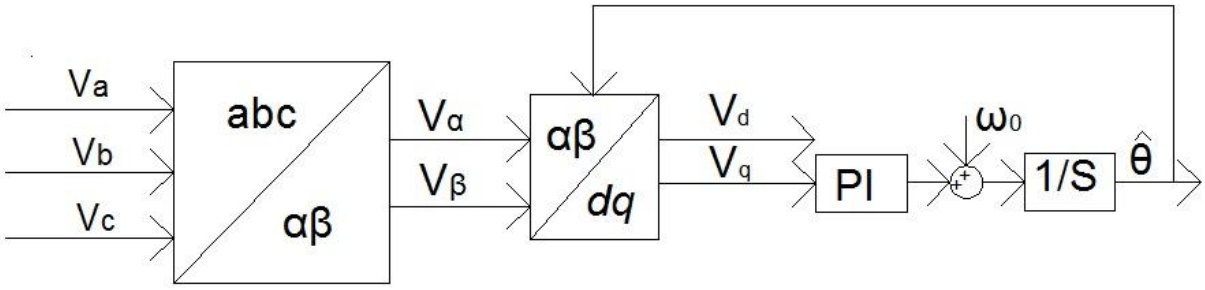

Fig.2.1. Basic block diagram of the conventional PLL

B. Double Synchronous Reference Frame (DSRF) PLL:

This method utilizes two synchronous reference frames similar to [12], i.e., the voltage vector v is decomposed into positive sequence phasor $v_+$and negative sequence phasorv_-, as shown in Fig. 2.3. In the general equation of $V_{\alpha\beta}$, α- and β-axis components both contain the information of the positive sequence and negative sequence which makes it difficult to detect the positive sequence component. A synthesis circuit, as shown in Fig. 2.2, is used to separate them. Then like two independent PLLs, the two synchronous reference frames rotating with the positive direction and negative direction respectively and detect the positive sequence and negative sequence components simultaneously [5].

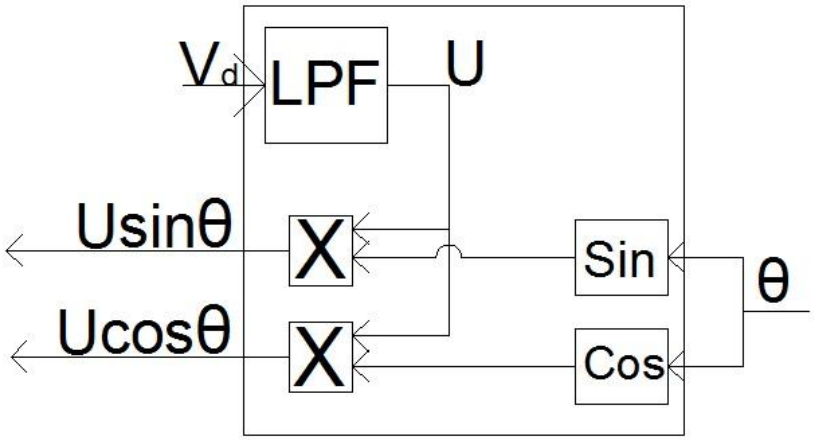

Fig. 2.2. Synthesis circuit

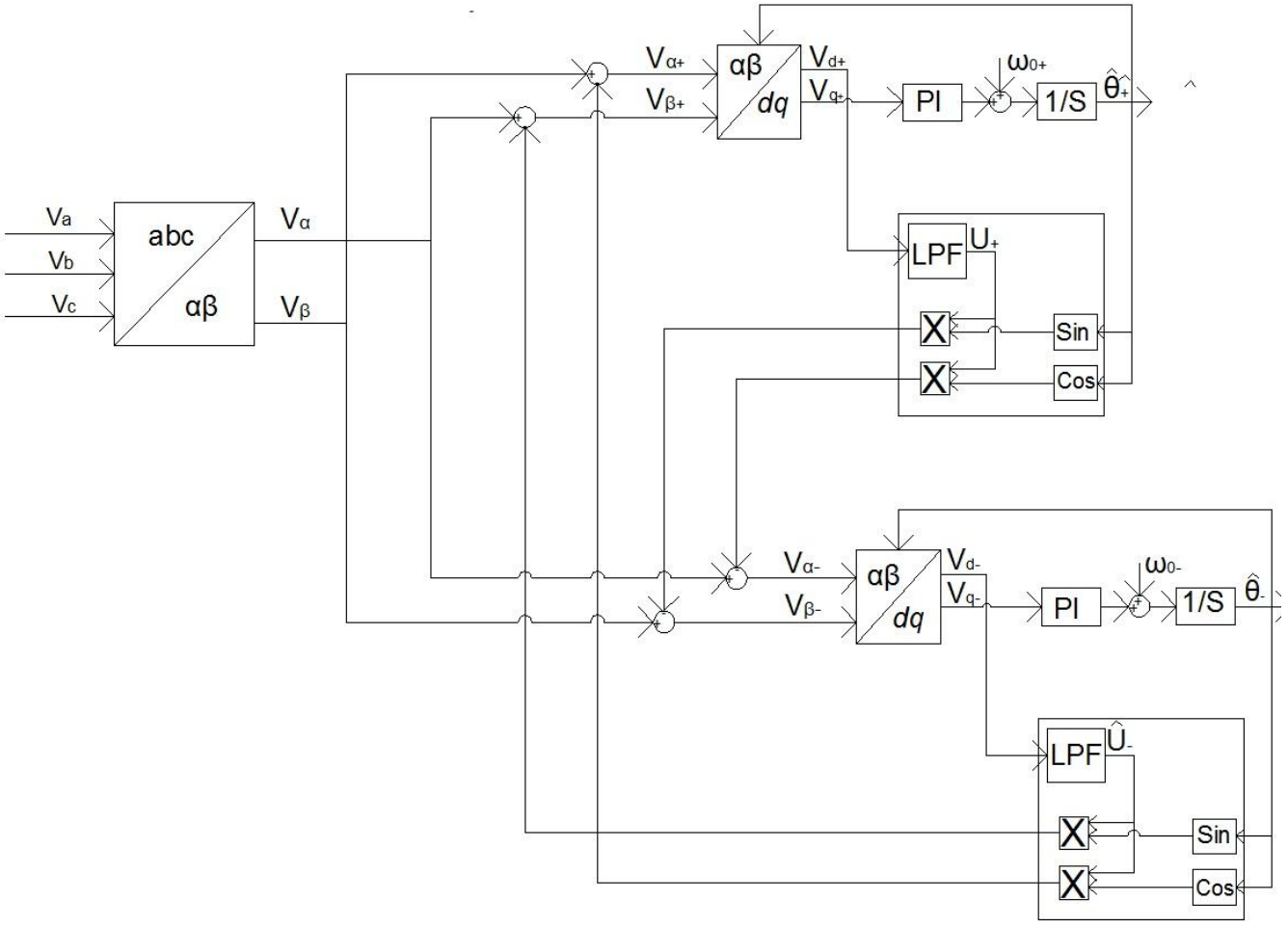

Fig.2.3. Basic block diagram of the DSRF PLL

C. Unbalanced Harmonic based (UH) PLL:

This work presents a PLL algorithm, referred as UH-PLL, able to provide an estimation of the angular frequency and both the positive and negative sequences of the fundamental component of an unbalanced distorted three-phase signal [13]. The main characteristics of the proposed UH-PLL scheme can be listed as follows:

(i) The UH-PLL includes a harmonic compensation mechanism to deal with the harmonic distortion present in the grid voltage.

(ii) The UH-PLL does not require transformation of variables into the synchronous reference frame coordinates as in conventional PLL schemes, but only transformation to fixed-frame coordinates.

(iii) The design of the UH-PLL is based on a more complete and generic model description of an unbalanced grid voltage signal distorted by low order harmonics.

(iv) The synchronization process in the UH-PLL is based on the detection of the fundamental frequency. The idea of using the frequency detection for grid synchronization has also been reported in [14], [15] and [16]. In other conventional PLL schemes the synchronization is based on the detection of the phase angle. But the objective of the proposed scheme is to deliver estimates for positive and negative sequences of the grid voltage, as well as an estimate of the fundamental frequency ω_0. For this, an adaptive estimator for state variables vαβ and ϕ αβ is designed based on the model considered in the next chapter.

As it will become clear later, the adaptive estimator generates two pairs of quadrature signals, and thus, it will be referred as the adaptive quadrature signals generator under unbalanced conditions (U-AQSG) [13].

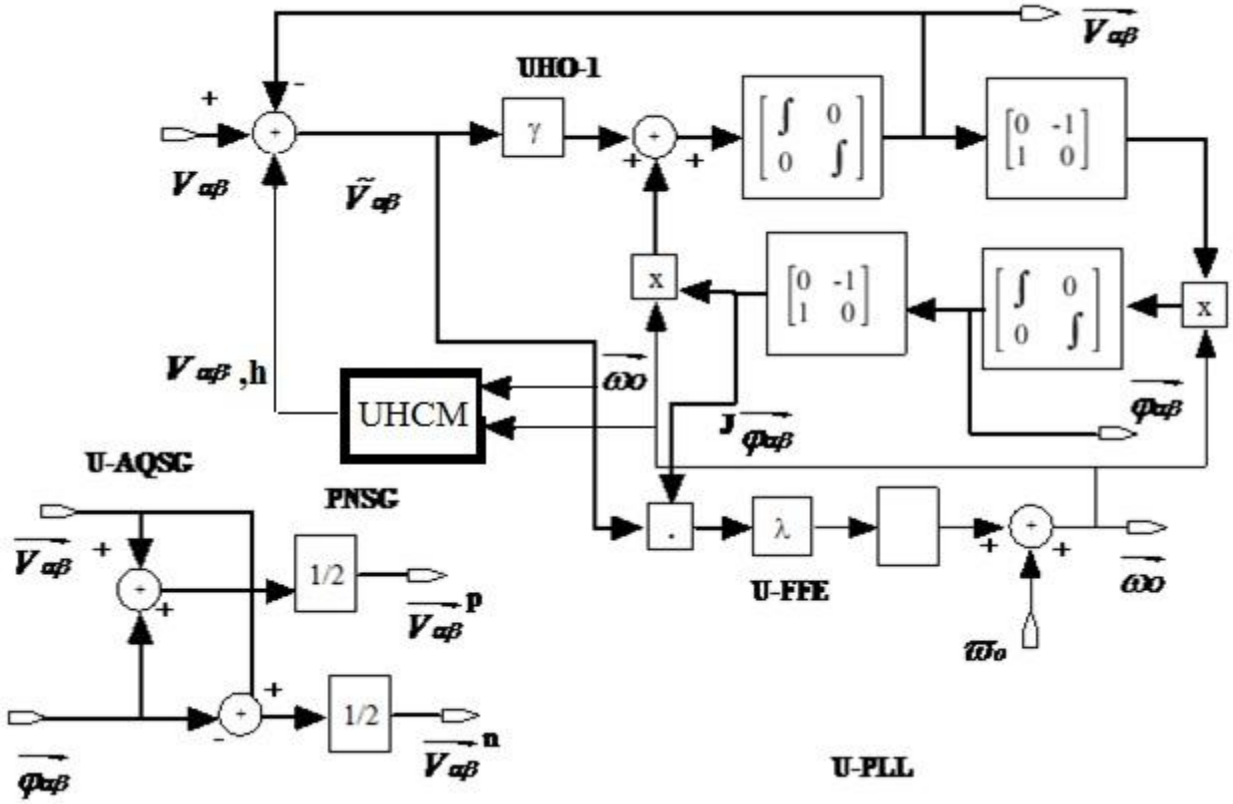

Fig. 2.4. Block diagram of the proposed UH-PLL algorithm including the harmonic compensation mechanism UHCM for an unbalanced and distorted reference signal $V_{\alpha\beta}$.

2.4 CONCLUSION:

The various grid synchronization algorithms have been studied. The earliest used phase detection method involves the concept of Zero Crossing Detector. Various kinds of PLL techniques are seen by their circuit models. The SRF PLL is used to detect the phase angle in case of 3-phase system. The DSRF PLL and UH PLL are used to decouple the positive and negative sequence components and to track the phase angle and angular frequency respectively for both the sequence components separately. The mathematical model of the PLLs and the corresponding phase detection results as obtained from MATLAB/SIMULINK environment are shown in the further chapters for better understanding.

CHAPTER 3

Grid Synchronizing Using Double Synchronous Reference Frame (DSRF) PLL

3.1 INTRODUCTION:

The method utilizes double rotating reference frames to transform the input signal and detects the positive fundamental component and negative sequence component simultaneously. It's based on a synthesis circuit which generates the orthogonal and in-phase signals to decouple input signal [5]. This method detects the phase angle without distortion even in variable-frequency environment compared to existing synchronization methods.

3.2 ANALYSIS OF SYNCHRONOUS REFERENCE FRAME (SRF) PLL:

Under ideal utility conditional, i.e., neither harmonic distortion nor unbalance, the d- and q-axis component can be express by:

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} cos\theta^{\wedge} & sin\theta^{\wedge} \\ -sin\theta^{\wedge} & cos\theta^{\wedge} \end{bmatrix} \begin{bmatrix} U\,cos\theta \\ U\,sin\theta \end{bmatrix} = \begin{bmatrix} U\cos(\theta - \theta^{\wedge}) \\ U\sin(\theta - \theta^{\wedge}) \end{bmatrix} \quad (3.1)$$

Where θ and $\theta^{\wedge}$ represent the phase of input signal and output of PLL respectively; U is the amplitude of input signal; V_d, V_q are the d- and q-axis component. As expressed in (3.1), q-axis component denotes the phase error and d-axis component will give the amplitude in the steady state. The transformation from abc to dq acts as a discriminator, and the structure of Fig. 2.1 is the PLL which can detect the phase [5]. Under unbalance utility conditions (without voltage harmonics), the voltage vector can be generically expressed as:

$$V = V_+ + V_- + V_0 \quad (3.2)$$

Where subscripts +, – and 0 define the vector for the positive, negative and zero sequence components. Using Clarke's transformation, the utility voltage vector is given by:

$$V_{\alpha\beta\gamma} = \begin{bmatrix} V_\alpha \\ V_\beta \\ V_\gamma \end{bmatrix} = T_{\alpha\beta/abc} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (3.3)$$

Where,

$$T_{\alpha\beta/abc} = \frac{2}{3}\begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad .$$

The zero-sequence component is on the γ-axis and has no influence on the following Park's transformation. Thus neglecting the zero-sequence component, the expression of the voltage vector on the αβ-plane is:

$$V_{\alpha\beta} = T_{\alpha\beta/abc}\,(V_+ + V_-) = \begin{bmatrix} U_+ \cos\theta_+ + U_- \cos\theta_- \\ U_+ \sin\theta_+ + U_- \sin\theta_- \end{bmatrix} \tag{3.4}$$

Where U and θ represent the vector amplitude and phase respectively. In (3.4), the voltage vector is no longer rotating with the positive direction and it has neither constant magnitude nor constant rotating frequency under unbalanced grid conditions. Therefore, in (3.5), after Park's transformation, q-axis component not only constitute of phase error but also 2ω ripple [5]. As shown in Fig.3.1, if a conventional PLL in Fig. 2.1 is used to detect the phase under unbalanced condition, the detected phase will be distorted, 2ω ripple in d- and q-axis component is so large and makes it difficult to get the information of phase error and amplitude [5].

$$V_{dq} = T_{dq/\alpha\beta}\ V_{\alpha\beta} = \begin{bmatrix} U_+\cos(\theta_+ - \hat{\theta}) + U_- \cos(\theta_- - \hat{\theta}) \\ U_+ \sin(\theta_+ - \hat{\theta}) + U_- \sin(\theta_- - \hat{\theta}) \end{bmatrix} \tag{3.5}$$

Where,

$$T_{dq/\alpha\beta} = \begin{bmatrix} cos\hat{\theta} & sin\hat{\theta} \\ -sin\hat{\theta} & cos\hat{\theta} \end{bmatrix}$$

ω is the angular frequency of voltage vector and $\hat{\theta} \approx \theta_+ = -\theta_- = \omega t$. To get a better estimation of the phase angle of positive-sequence voltage component, the control-loop bandwidth has to be reduced in order to avoid the appearance of double frequency oscillation term, but the dynamic response will be deteriorated and the detected positive-sequence voltages are distorted and unbalanced [17].

The results obtained from simulation of SRF PLL during unbalanced grid voltage are shown in Fig. 3.1. Fig. 3.1 (a) shows the 3-phase unbalanced grid voltage such that phase a magnitude is greater than the other 2 phases. As obtained in equation 3.4, the d and q axis voltages are not constant, rather it contains second harmonic ripples. Fig.3.1 (b) shows these second harmonic

components in d axis and q axis volt ages. This sinusoidal nature in q axis voltage affects the output of PI controller and generates sinusoidal error signal and hence sinusoidal angular frequency (at central frequency ω_0 i.e.100π in this case) this is shown in Fig. 3.1 (b). From Fig. 3.1 (c), it can be seen that, the detected phase obtained by the time integration of angular frequency is not perfectly triangular but rather contains sinusoidal variations. Thus it can be seen from the graph that SRF PLL fails to track the phase angle properly during unbalanced grid conditions.

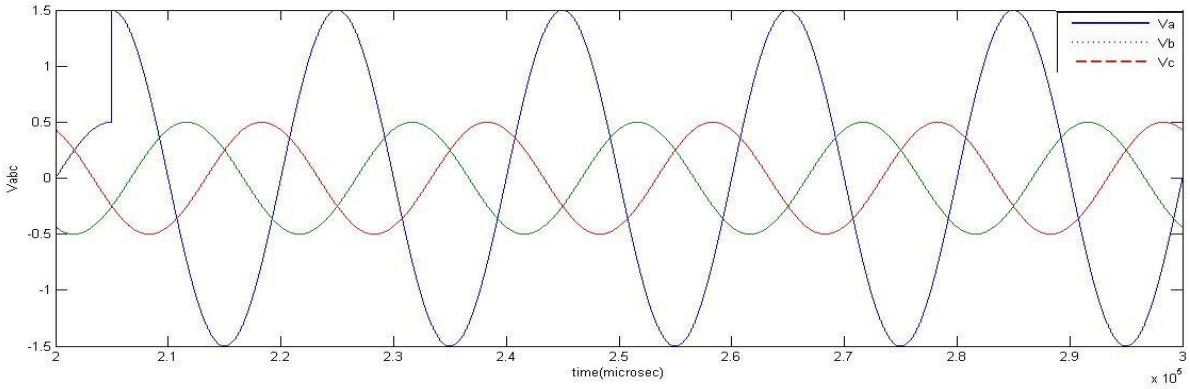

Fig. 3.1 (a)

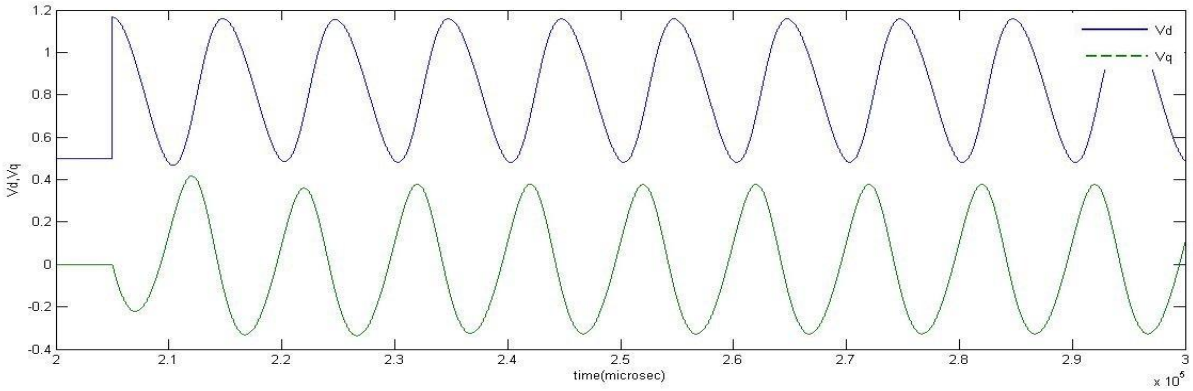

Fig. 3.1 (b)

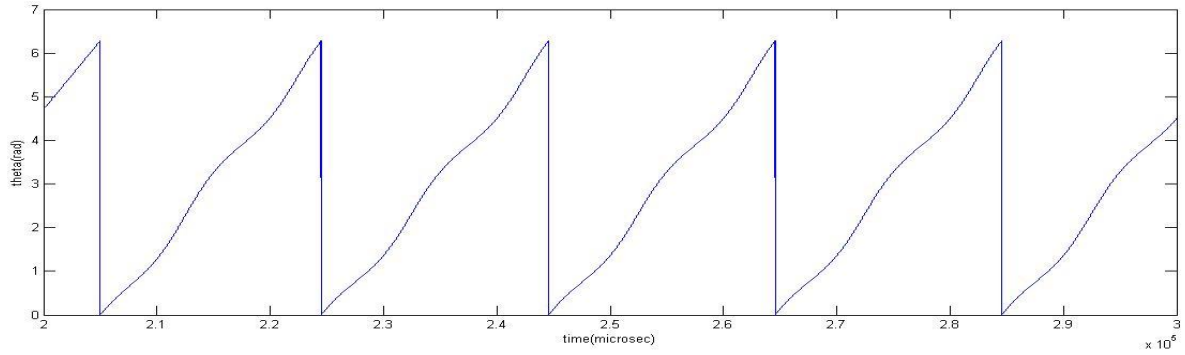

Fig. 3.1 (c)

Figure 3.1: Simulation Results for SRF PLL during Unbalanced Grid Conditions (a) Grid Voltage Waveform (b) d-q Components of Grid Voltage (c) Detected Phase Angle.

3.3 ANALYSIS OF DOUBLE SYNCHRONOUS REFERENCE FRAME (DSRF) PLL:

The synthesis circuit importing d-axis component from Park's transformation which is the voltage vector amplitude in the steady state and detected phase generates orthogonal signal and in-phase signal. It consists of a low-pass filter (LPF), two multipliers and two orthogonal trigonometric functions [5]. Because the phase comes from the PLL output, the two signals, which is obtained from the trigonometric function of the input signal phase will be orthogonal and in-phase with input respectively. Then by multiplying the amplitude, the synthesis circuit generates two orthogonal signals. These generated orthogonal signals are used to decouple the signals in (3.4), as shown in Fig.2.3.Subscripts + and – represent the coefficient for the positive and negative respectively.

There are two PLLs including two synthesis circuits in the structure. This DSRF PLL detect the positive and negative sequence component at the same time. As shown in Fig.2.3, the input signals of each Park's transformation, vαand vβ, are calculated by subtracting the generated signals of others [5]. In this way, after a transient process, the input signals of each PLL are cleaned up, and the distortion is canceled at the output of both PLL's i.e. for positive and sequence components.

The PLL with initial angular frequency ω_{0+} detects the positive sequence component and PLL with ω_{0-} detects the negative sequence component.

In the initial state, v_d is zero, $\theta^{\wedge}$ is $\omega_0 t$, the output of synthesis circuit are all equal to zero, which means decoupling circuit has no effect and each PLLs contains both positive sequence and negative sequence components. The rotating reference frame rotating with positive direction gives rise to (3.6) after Park's transformation

$$\begin{bmatrix} V_{d+} \\ V_{q+} \end{bmatrix} = \mathrm{U}_+ \begin{bmatrix} \cos(\theta_+ - \theta^{\wedge}_+) \\ \sin(\theta_+ - \theta^{\wedge}_+) \end{bmatrix} + \mathrm{U}_- \begin{bmatrix} \cos(\theta_- - \theta^{\wedge}_-) \\ \sin(\theta_- - \theta^{\wedge}_-) \end{bmatrix} \tag{3.6}$$

$\theta^{\wedge}_+$ is set to $\omega_{0+} t$ in Fig.2.3 at initial state, where ω_{0+} is approximate the center angular frequency of positive sequence component.

Then (3.6) can be rewritten as:

$$\begin{bmatrix} V_{d+} \\ V_{q+} \end{bmatrix} = \begin{bmatrix} \mathrm{U}_+ + \mathrm{U}_- \cos(-2\omega_{0+}\mathrm{t}) \\ \mathrm{U}_- \sin(-2\omega_{0+}\mathrm{t}) \end{bmatrix} \tag{3.7}$$

There is 2ω ripple including in the d-axis component, so a low-pass filter (LPF) is need to attenuate ripple and help the PLL to get stable. In Fig. 2.2, LPF block is low-pass filter, it can be defined as:

$$\mathrm{LPF(S)} = \frac{\omega_c}{s+\omega_c} \tag{3.8}$$

Where ω_c determines the cut-off frequency of LPF.

In order to analyze the behavior of proposed PLL. The state equations can be derived from Fig. 2.2 [5].

$$\left.\begin{aligned} \dot{x}_1 &= \omega_c(\mathrm{U}_+ - x_1 + (\mathrm{U}_- - x_2)\cos(\theta_+ - \theta_-)) \\ \dot{x}_2 &= \omega_c(\mathrm{U}_- - x_2 + (\mathrm{U}_+ - x_1)\cos(\theta_+ - \theta_-)) \end{aligned}\right\} \tag{3.9}$$

Where $\begin{cases} \dot{x}_1 = \mathrm{U}_+ \\ \dot{x}_2 = \mathrm{U}_- \end{cases}$

In (3.9), when the state variables get into steady state, there will be x_1=U_+ and x_2=U_- .That is, the d-axis component will converge to input voltage vector amplitude after some time, and synthesis

circuit start to output decoupling signals [5]. At last the input of each PLL will be

$$\left.\begin{aligned} V_{\alpha+} &= V_{\alpha} - \mathrm{U}_{-}\cos\theta_{-} = \mathrm{U}_{+}\cos\theta_{+} \\ V_{\beta+} &= V_{\beta} - \mathrm{U}_{-}\sin\theta_{-} = \mathrm{U}_{+}\sin\theta_{+} \end{aligned}\right\} \tag{3.10}$$

$$\left.\begin{aligned} V_{\alpha-} &= V_{\alpha} - \mathrm{U}_{+}\cos\theta_{+} = \mathrm{U}_{-}\cos\theta_{-} \\ V_{\beta-} &= V_{\beta} - \mathrm{U}_{+}\sin\theta_{+} = \mathrm{U}_{-}\sin\theta_{-} \end{aligned}\right\} \tag{3.11}$$

In (3.10) and (3.11), a conventional PLL in Fig.2.1 is enough to detect the phase. Positive sequence component phase comes from (3.10) and negative sequence component phase comes from (3.11). In (3.9), variable ω_c determines the convergence speed. The bigger ω_c is, the faster their convergence speeds are. But it's important to note that the LPF is used to attenuate the 2ω ripple which means ω_c should not be bigger than $2\omega_0$, otherwise, the system may become unstable. A trade-off must be made between speed and stability in order to achieve the desired behavior. The LPF isn't included in the closed-loop of PLL, so that it's bandwidth doesn't affect the bandwidth of PLL [5]. Also the LPF is only useful in the dynamic process to help the system get into stable operation. In the steady state, each PLL's input signals are balanced and no 2ω ripple appears in d- or q-axis component, LPF merely attenuate noise.

For a conventional PLL, the small signal model has already been analyzed in [17-19]. If the parameters of PI controller are chosen carefully, the PLL can be stable and can obtain input signal phase angle. Therefore, the proposed PLL can be stable and can detect the voltage phase and amplitude without distortion. As an additional function, negative sequence component is detected too. Because synthesis circuit utilizes the phase of PLL itself, the generated signals are frequency adaptive. The MATLAB results obtained for DSRF PLL under various abnormal grid conditions are discussed in this section.

3.3.1 Response of DSRF PLL During Unbalanced Grid Voltages

The dynamic responses obtained from simulation for DSRF PLL during unbalance grid voltage are shown in Fig. . The PI tuning used for these results are K_p = 2 and K_i=0.002.

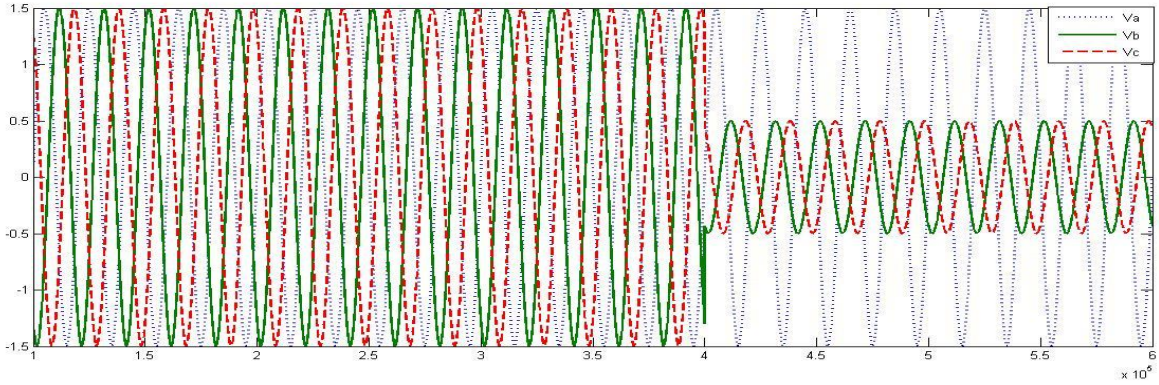

Fig.3.2 (a)

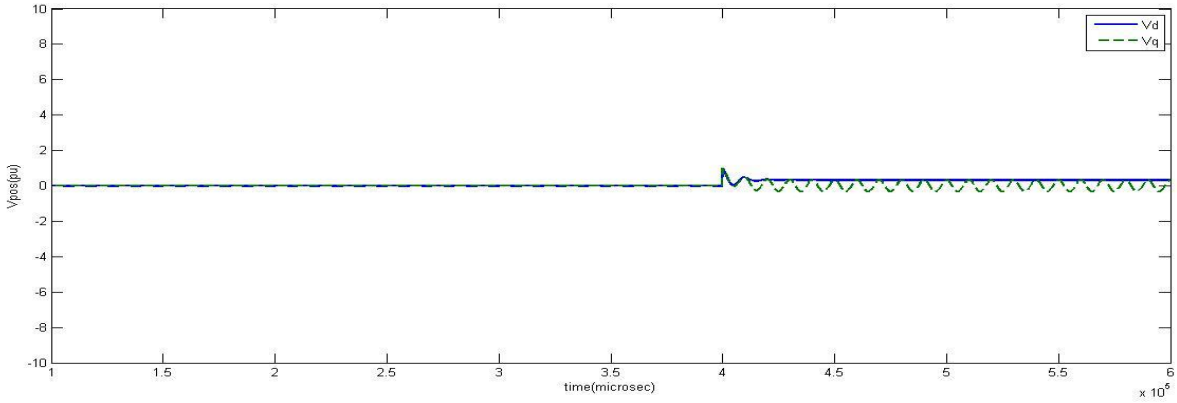

Fig.3.2(b)

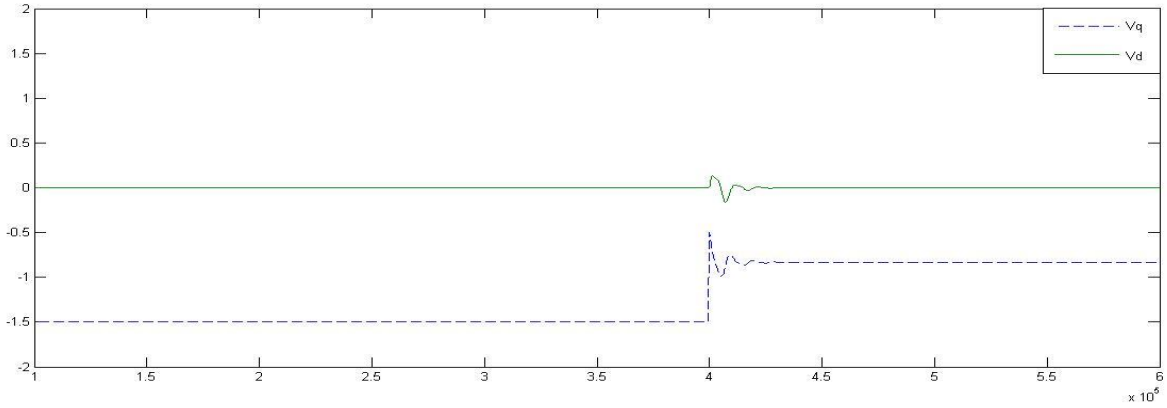

Fig.3.2 (c)

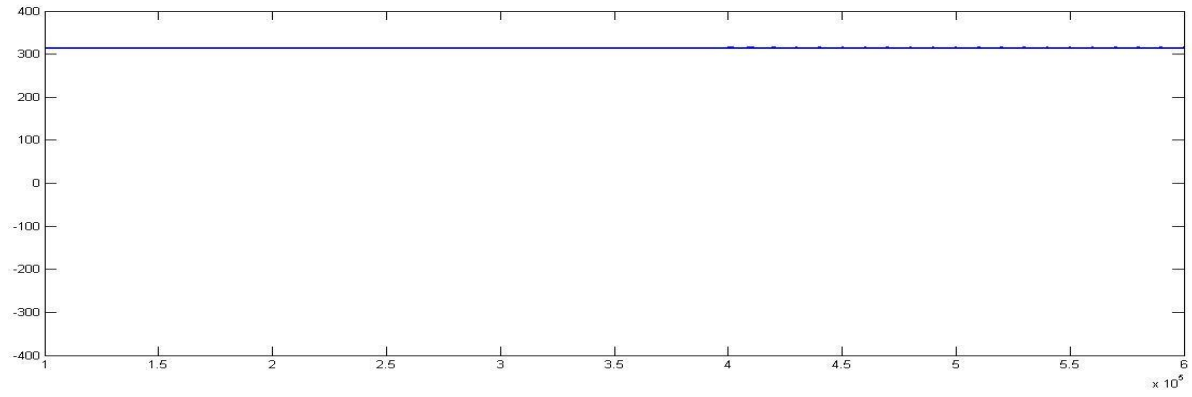

Fig.3.2 (d)

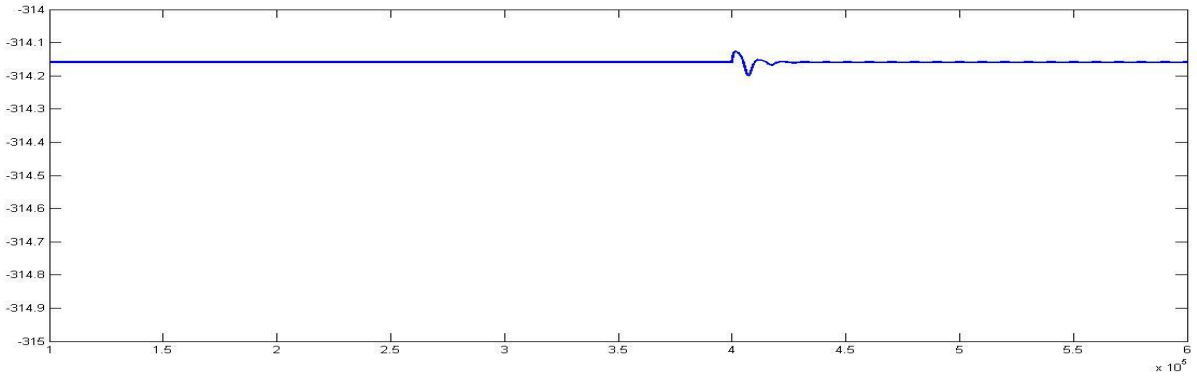

Fig.3.2 (e)

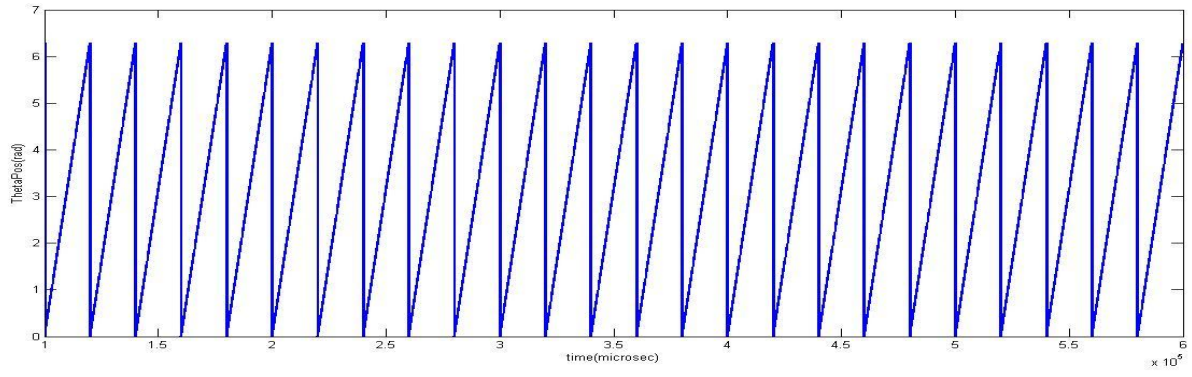

Fig.3.2 (f)

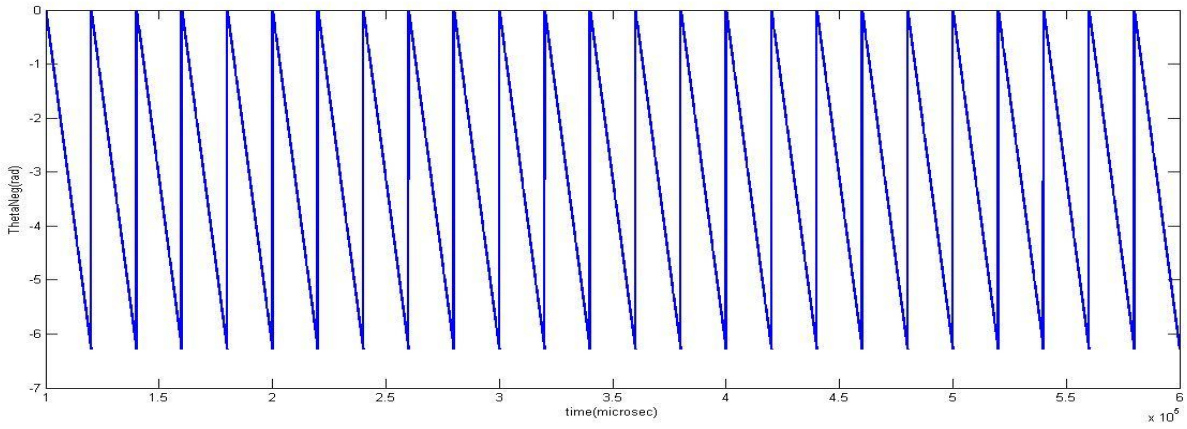

Fig.3.2 (g)

Figure 3.2: Dynamic Response of DSRF PLL during Unbalanced Grid Conditions (a) Grid Voltage Waveforms (b) d axis and q axis Voltage of Positive Sequence Component (c) d axis and q axis Voltage of Negative Sequence Component (d) Detected Angular Frequency of Positive Sequence Component (e) Detected Angular Frequency of Negative Sequence Component (f) Detected Phase Angle of Positive Sequence Component (g) Detected Phase Angle of Negative Sequence Component.

Fig.3.2 (a) shows a 3-phase signal which remains balanced up to time t=0.4 sec and then voltage amplitude of 2 of the phases reduces to 0.5 from their initial value of 1.5.The dynamic responses are observed for this input. As shown in Fig.3.2 (b) d axis voltage of positive sequence component is almost constant both during balanced and unbalanced period and negligible sinusoidal variations are observed during the transient period (from t=0.4 to 0.42 sec). Similarly as shown in Fig.3.2(c) the d axis voltage of negative sequence component is also almost constant having negligible variations. As shown is Fig. 3.2(b) the q axis voltage of the positive sequence component maintains mostly a constant value both in balanced and unbalanced conditions. The transients observed when there is sudden change in input voltage (at t=0.4 sec). The transient vanishes to give a nearly constant value (nearly at zero) for q axis voltage of positive sequence component. A similar nature is observed for q axis voltage of negative sequence component as seen in Fig. 3.2 (c).The angular frequencies of positive and negative sequence components are both similar to their respective q axis voltages and hence a nearly constant angular frequency is observed for positive and negative sequence components with small distortion for a transient period (Fig. 3.2(d) and Fig. 3.2(e) respectively). For these constant angular frequencies we observe perfectly triangular phase

angle detection for positive sequence (Fig. 3.2(f)) and negative sequence (Fig. 3.2(g)). The detected phase angle varies linearly every cycle from 0 to 2π for positive sequence and 0 to -2π for negative sequence.

3.3.2 Response of DSRF PLL for a Line to Ground Fault

The results obtained from simulation of DSRF PLL under line to ground fault are shown in Fig. 3.3. The tuning used for these results are Kp = 2 and Ki=0.002.

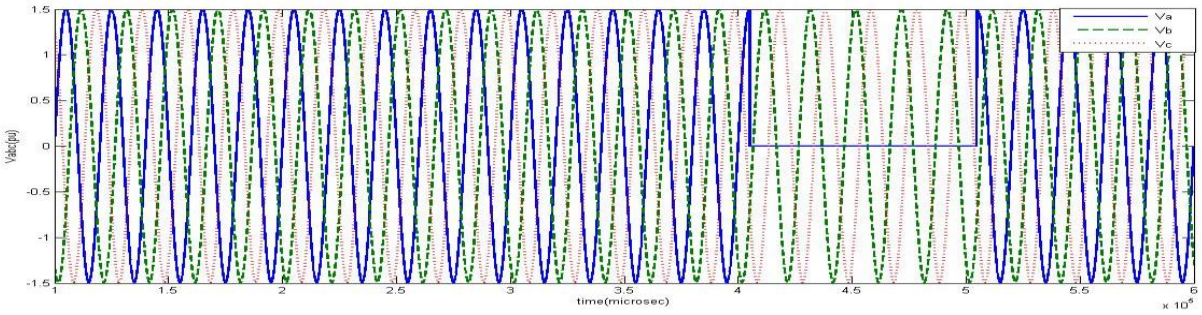

Fig.3.3 (a)

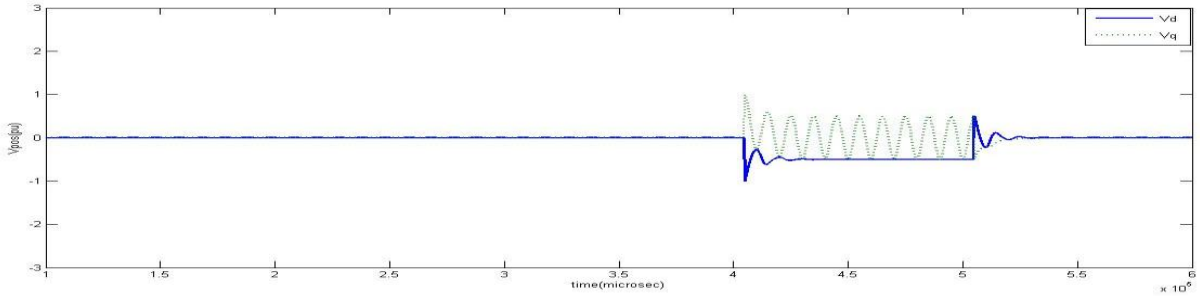

Fig.3.3 (b)

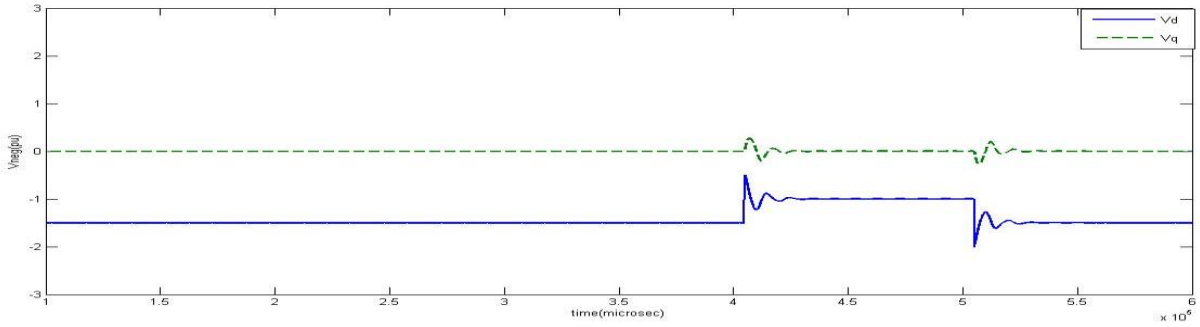

Fig.3.3 (c)

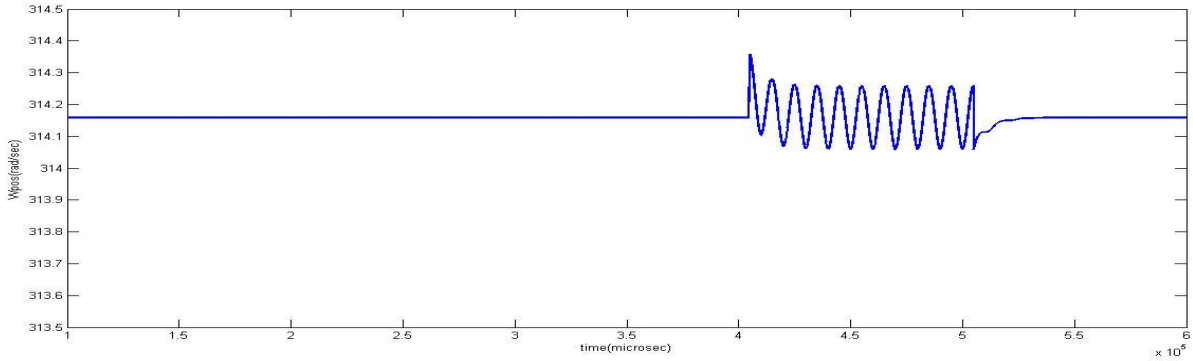

Fig.3.3 (d)

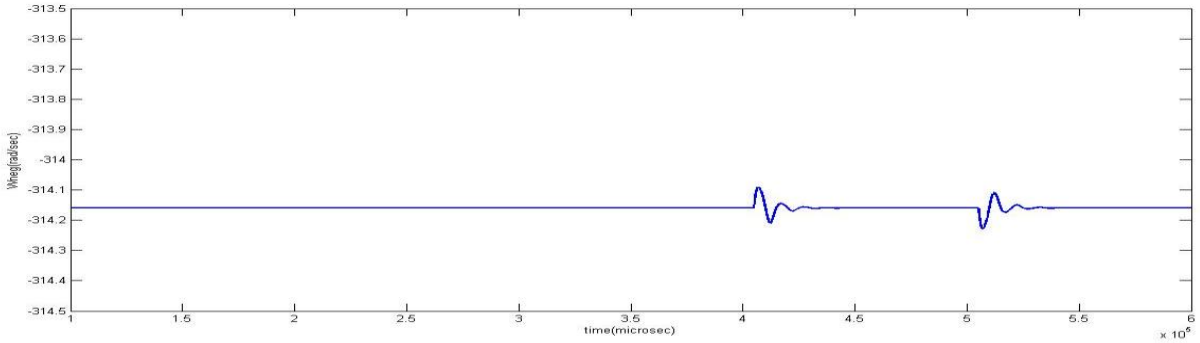

Fig.3.3 (e)

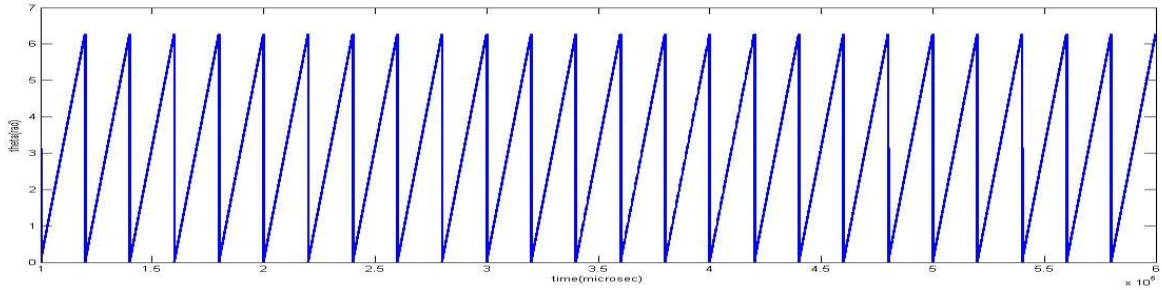

Fig.3.3 (f)

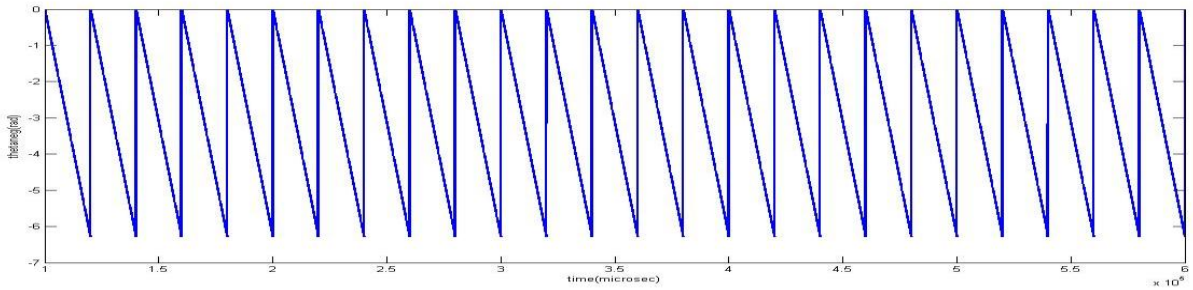

Fig.3.3 (g)

Figure 3.3: Response of DSRF PLL under Line to Ground Fault (a) Grid Voltage Waveforms (b) d axis and q axis Voltage of Positive Sequence Component (c) d axis and q axis Voltage of Negative Sequence Component (d) Detected angular Frequency of Positive Sequence Component (e) Detected Angular Frequency of Negative Sequence Component (f) Detected Phase Angle of Positive Sequence Component (g) Detected Phase Angle of Negative Sequence Component.

Fig.3.3 (a) shows the voltage waveform when line to ground fault occurs. The system was initially in balanced condition (with amplitude 1.5V). Line to ground fault occurs at time, t = 0.4sec. At this instant the phase voltage of one of the phases reduces and remains at an amplitude of zero due to a line to ground fault, while the other two phases remain undisturbed. The system regains its balanced state at time, t = 0.5 sec. The d axis voltage of positive sequence component shown in Fig.3.3 (b) is constant at the amplitude of the signals during balanced input. During line to ground fault, the d axis voltage reduces and some oscillations with very small amplitude are observed. The d axis voltage of negative sequence component (Fig.3.3(c)) also maintains its constant value other than very small transients that occur at time t = 0.4 sec and 0.5 sec. The q axis voltages of positive sequence (Fig 3.3(b)) and negative sequence (Fig.3.3 (c)) maintains their near zero value at all instants, with some oscillations at the instants during which switching of voltages occur. The angular frequencies of positive sequence and negative sequence components maintain their constant value at 100π and -100π with small distortions (Fig. 3.3 (d) and Fig. 3.3(e) respectively).Therefore the detected phase angle is perfectly triangular for both positive (Fig. 3.3(f)) and negative sequence (Fig. 3.3(g)).

3.3.3 Response of DSRF PLL During Voltage Sag

The simulation results obtained for DSRF PLL during voltage sag are shown in Fig. 3.5. The PI tuning used for these results are Kp = 2 and Ki=0.002.

As shown in Fig. 3.4(a), voltage sag occurs at time t = 0.3 sec when all the three phase voltages reduces to 1.25V from their initial voltage of 1.5V. The three phases regain their original value of 1.5V at time t = 0.4 sec. This kind of sudden reduction in voltage for small period (2 and half cycles in this case) is known as voltage sag. Fig.3.4 (b) illustrates the d axis voltage of positive sequence component, which is constant at the amplitude of the input signal.

In the duration when voltage sag occurs, the d axis voltage remains constant but its value changes to the new amplitude. Similarly as shown in Fig.3.4 (c) the d axis voltage of negative sequence component also maintains its constant zero value. The same holds good for q axis voltage of negative sequence component which remains constant at 1.6v in both the periods (Fig. 3.4(c)). As q axis voltages are constant the corresponding angular frequency for both positive and negative components maintains their constant value at 100π and -100π with small distortions (Fig. 3.4(d) and Fig. 3.4(e)).The detected phase for both the sequence components is perfectly triangular because of the constant angular frequency observed (Fig. 3.4 (f) and Fig. 3.4(g)).

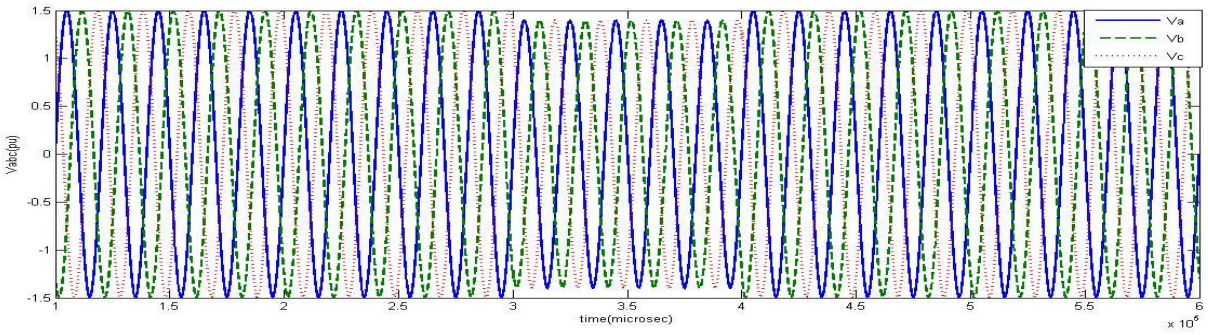

Fig.3.4 (a)

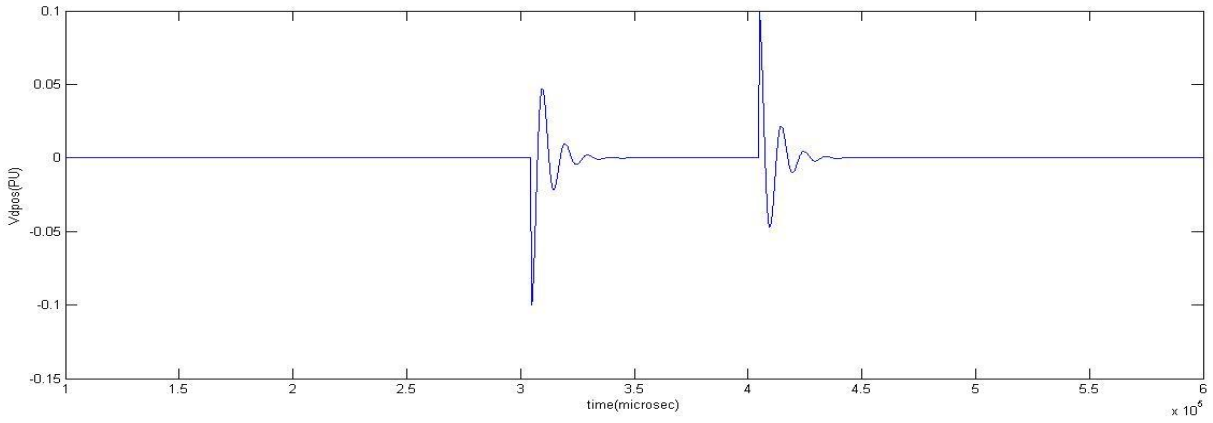

Fig.3.4(b)

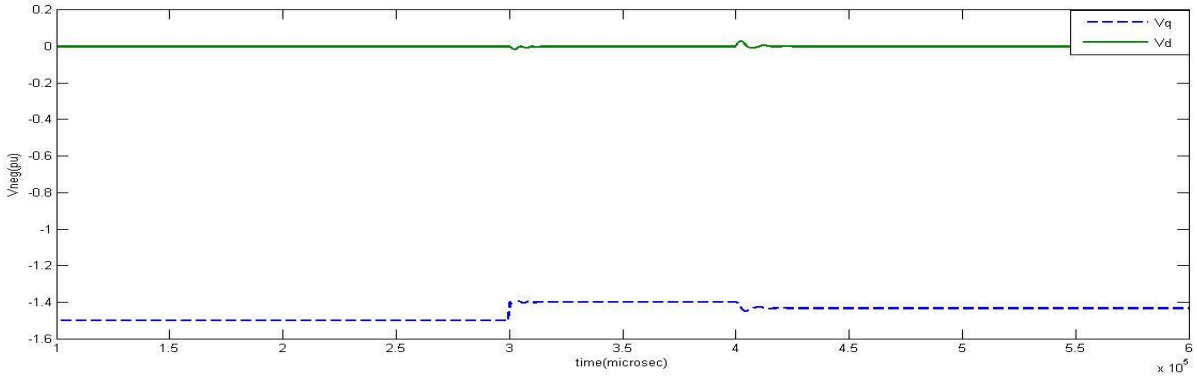

Fig.3.4(c)

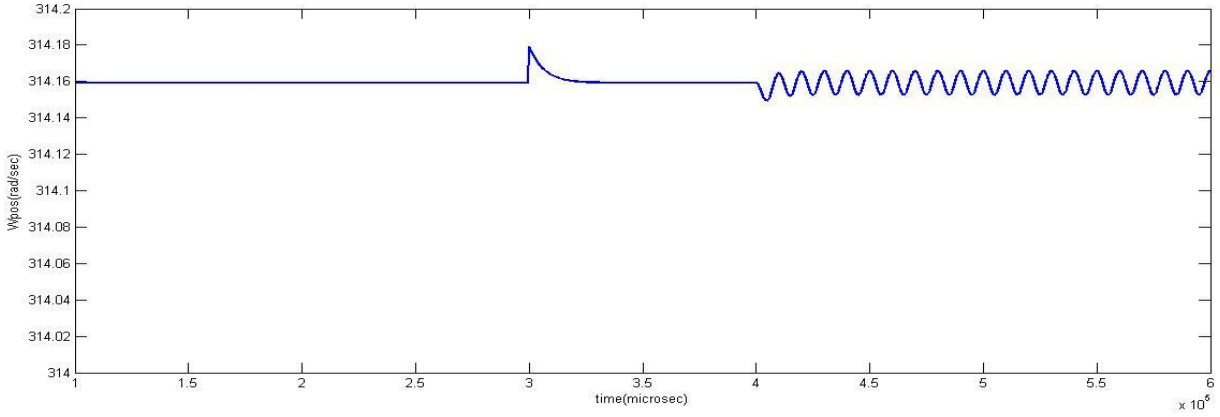

Fig.3.4(d)

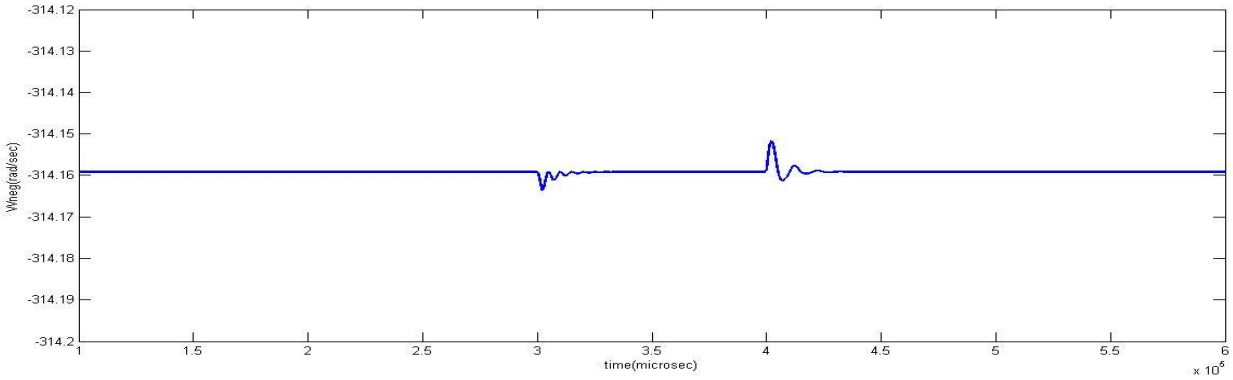

Fig.3.4(e)

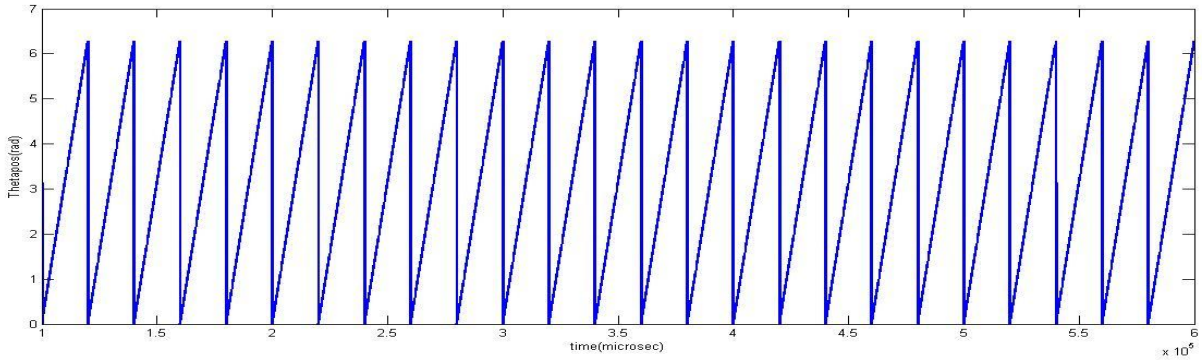

Fig.3.4(f)

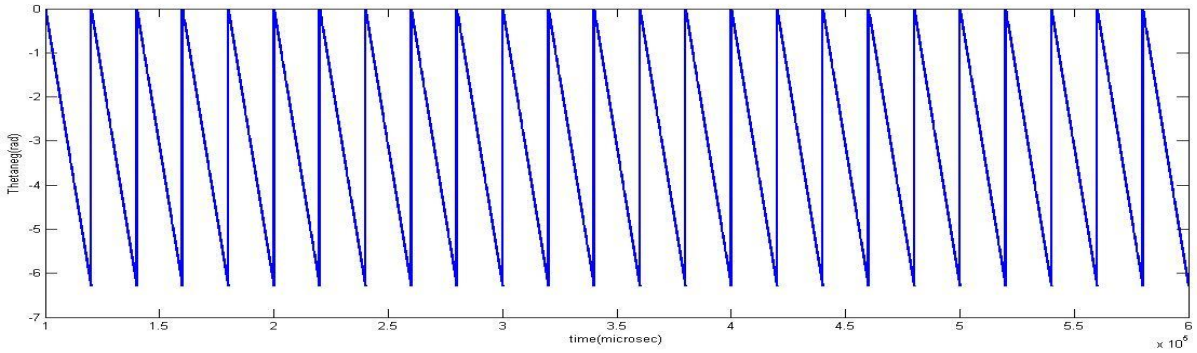

Fig.3.4(g)

Figure 3.4: Response of DSRF PLL during Voltage Sag (a) Grid Voltage Waveforms (b) d axis Voltage of Positive Sequence Component (c) d axis and q axis Voltage of Negative Sequence Component (d) Detected Angular Frequency of Positive Sequence Component (e) Detected Angular Frequency of Negative Sequence Component (f) Detected Phase Angle of Positive Sequence Component (g) Detected Phase Angle of Negative Sequence Component.

3.4 CONCLUSION:

The chapter presents the performance of Double Synchronous Reference Frame (DSRF) PLL for phase detection under abnormal grid conditions. The abnormal grid conditions include line to ground fault and the various quality problems include voltage sag, frequency deviation and voltage dip. From the above discussions we can conclude that the studied DSRF PLL can accurately detect the phase angle irrespective of the grid conditions. Moreover, the DSRF PLL can also decouple the positive and negative sequence components of grid voltages in order to ensure sinusoidal current injection into the grid. Further, the obtained results clearly show that the DSRF PLL gives better response in tracking the positive sequence component over the conventional SRF PLL which fails to track the phase angle whenever there is an unbalance in the grid.

CHAPTER 4

Analysis of Unbalanced Harmonic (UH) Based PLL

4.1 INTRODUCTION:

A brief introduction to the UH PLL has already been mentioned in section 2.3.2(C). The detailed mathematical analysis of this PLL has been done in this chapter. The response of this PLL is studied for different abnormal grid conditions like voltage unbalance, harmonic injection. With the help of these results the perfect tracking of angular frequency by UHPLL is shown and explained.

4.2 Analysis Of Unbalanced and Harmonic based PLL:

This section presents the model for the grid voltage, which is essential for the design of the UH-PLL. For a clear presentation, only the unbalance operation case is treated first, without harmonics, from which a basic scheme referred as U-PLL is presented [13]. Then, the effects of the harmonic distortion are included, which results in the addition of the UHCM to the basic model. This more complete scheme is thus referred as the UH-PLL.

4.2.1 Grid Voltage Under Unbalanced Condition:

A model describing the grid voltage signal is presented [13]. This signal is originally described in three-phase coordinates $\mathbf{V}_{123} = [v1, v2\ v3]^T$. The grid voltage signal is transformed to (fixed-frame) αβ-coordinates using Clarke's transformation. Moreover, both positive and negative sequences are considered to deal with the unbalanced case.

$$V_{\alpha\beta} = V^{p}_{\alpha\beta} + V^{n}_{\alpha\beta} = e^{J\theta} V^{p}{}_{dq} + e^{-J\theta} V^{n}{}_{dq} \tag{4.1}$$

$$e^{J\theta} = \begin{bmatrix} cos\theta_0 & sin\theta_0 \\ -sin\theta_0 & cos\theta_0 \end{bmatrix}, \qquad J = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \tag{4.2}$$

Where $V^{p}_{\alpha\beta}$ and $V^{n}_{\alpha\beta}$ represent the positive and negative symmetric components of $V_{\alpha\beta}$ respectively. Based on this, the following model that completely describes the unbalanced sinusoidal signal generator $V_{\alpha\beta}$ is obtained as

$$\dot{V}_{\alpha\beta} = \omega_0 J \varphi_{\alpha\beta} \tag{4.3}$$

$$\dot{\varphi}_{\alpha\beta} = \omega_0 J V_{\alpha\beta} \tag{4.4}$$

Where ω_0 represents the fundamental frequency of the grid voltage and the following auxiliary variable has been defined, which is necessary to complete the model.

$$\varphi_{\alpha\beta} \cong V^p_{\alpha\beta} - V^n_{\alpha\beta} \tag{4.5}$$

Notice that (4.3)-(4.4) represents the model of an oscillator generating an unbalanced sinusoidal signal, therefore, it is referred as the unbalanced harmonic oscillator (UHO) [13]. Based on definitions of vαβ in (4.1) and of ϕαβ in (4.5), it is possible to establish the following relationship

$$\begin{bmatrix} V_{\alpha\beta} \\ \varphi_{\alpha\beta} \end{bmatrix} = \begin{bmatrix} I_2 & I_2 \\ I_2 & -I_2 \end{bmatrix} \begin{bmatrix} V^p_{\alpha\beta} \\ V^n_{\alpha\beta} \end{bmatrix} \tag{4.6}$$

Where I_2 is the 2×2 Identity matrix.

4.2.2 Model Of The Grid Voltage Considering Harmonic Distortion:

In the case of the presence of harmonic distortion in the grid voltage, the previous description (4.1) can be represented as follows

$$V_{\alpha\beta} = \sum_{K\in\{H\}} (V^p_{\alpha\beta,k} + V^n_{\alpha\beta,k}) = \sum_{K\in\{H\}} (e^{JK\theta} V^p_{dq,k} + e^{-JK\theta} V^n_{dq,k}) \tag{4.7}$$

$$e^{JK\theta} = \begin{bmatrix} cosk\theta_0 & sink\theta_0 \\ -sink\theta_0 & cosk\theta_0 \end{bmatrix} \tag{4.8}$$

As before it is possible to establish the following relationship for the fundamental component

$$\begin{bmatrix} V_{\alpha\beta,1} \\ \varphi_{\alpha\beta,1} \end{bmatrix} = \begin{bmatrix} I_2 & I_2 \\ I_2 & -I_2 \end{bmatrix} \begin{bmatrix} V^p_{\alpha\beta,1} \\ V^n_{\alpha\beta,1} \end{bmatrix} \tag{4.9}$$

4.2.3 BASIC U-PLL FOR UNBALANCED OPERATION:

The objective of the proposed scheme is to deliver estimates for positive and negative sequences of the grid voltage, as well as an estimate of the fundamental frequencyω_0 . For this, an adaptive

estimator for state variables $V_{\alpha\beta}$ and $\varphi_{\alpha\beta}$ is designed based on the model. The adaptive estimator generates two pairs of quadrature signals, and thus, it will be referred as the adaptive quadrature signals generator under unbalanced conditions (U-AQSG) [13].

(i) **Adaptive quadrature signals generator U-AQSG:**

The estimator U-AQSG is proposed for the estimation of the fundamental component of state variables $V_{\alpha\beta}$ and $\varphi_{\alpha\beta}$. Where γ is a positive design parameter used to get the required damping, and $\widehat{\omega_0}$ is the estimate of the unknown parameter ω_0 [13]. The U-AQSG consists of the similar system model (4.3)-(4.4) to which a damping term is added, that is,

$$\dot{\widehat{V}}_{\alpha\beta} = \widehat{\omega_0}\mathrm{J}\,\hat{\varphi}_{\alpha\beta} + \gamma_1\tilde{V}_{\alpha\beta} \tag{4.10}$$

$$\dot{\hat{\varphi}}_{\alpha\beta} = \widehat{\omega_0}\mathrm{J}\,\hat{V}_{\alpha\beta} \tag{4.11}$$

(ii) **Fundamental Frequency Estimator – U-FFE :**

The reconstruction of $\widehat{\omega_0}$ involved in (4.10)-(4.11) is performed by means of the following adaptive law referred as the fundamental frequency estimator (U-FFE).

$$\dot{\widehat{\omega}} = \lambda\tilde{V}_{\alpha\beta}{}^{T}\mathrm{J}\hat{\varphi}_{\alpha\beta} \tag{4.12}$$

Where λ >0 is the adaptation gain and J was defined in (4.2).

The design of this estimator follows the estimation by using Lyapunov's approach.

(iii) **Positive and negative sequences generator – PNSG:**

Having the estimates $\hat{V}_{\alpha\beta}$ and $\hat{\varphi}_{\alpha\beta}$ coming out of estimator (4.10)-(4.11), and based on relationship (4.6), the positive and negative sequences of the grid voltage can now be reconstructed as follows

$$V^{p}_{\alpha\beta} = \frac{1}{2}\left(\hat{V}_{\alpha\beta} + \hat{\varphi}_{\alpha\beta}\right) \tag{4.13}$$

$$V_{\alpha\beta}^{n} = \frac{1}{2}(\hat{V}_{\alpha\beta}\text{-}\hat{\varphi}_{\alpha\beta}) \tag{4.14}$$

Which is referred as the positive and negative sequences generator (PNSG). Summarizing, the proposed U-PLL consists of the U-AQSG (4.10)-(4.11), U-FFE (4.12), and the PNSG (4.13)-(4.14). A block diagram of the proposed U-PLL algorithm is depicted in Fig.4.1. Notice that in the U-FFE a feed forward term has been included that prevents transients during the startup operation. In this diagram all thick lines represent vector variables, while normal lines represent scalar variables [13]. Notice also that the U-AQSG is composed by a basic block referred as the unbalanced harmonic oscillator (UHO-1), whose output is compared to the measured voltage signal and the error is fed back to it [13].

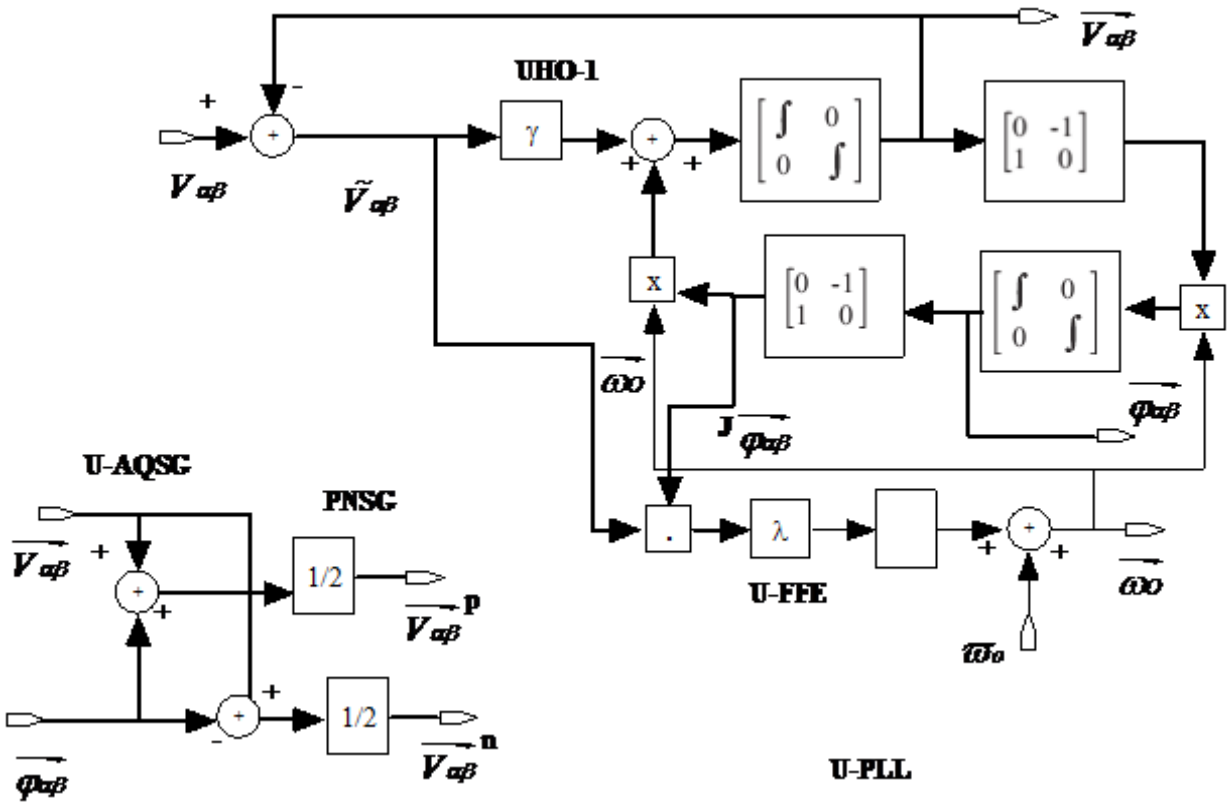

Fig. 4.1. Block diagram of the proposed U-PLL algorithm considering a sinusoidal unbalanced reference signal $V_{\alpha\beta}$[13].

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4.2.4 PROPOSED UH-PLL CONSIDERING UNBALANCE AND HARMONIC DISTORTION

The previous scheme U-PLL is extended to consider harmonic distortion present in the grid voltage. For this purpose it is proposed to introduce a harmonic compensation mechanism (UHCM) as shown in Fig. 2.3. The scheme is referred as UH-PLL as it considers the operation under unbalanced and harmonic distortion. Previous algorithms in [13] and [20] did not include any explicit mechanism for harmonic cancelation. And thus a slight ripple was present in the responses. This effect could be alleviated by limiting the bandwidth of the overall scheme, however, the speed of response is reduced. Hence a tradeoff between the speed of response and the harmonic compensation properties was established. In the UH-PLL scheme this tradeoff is relaxed by the introduction of the UHCM, which allows fast and clean responses.

4.2.5 Unbalanced Harmonic Compensation Mechanism – UHCM

The idea behind the UHCM consists of designing an estimator to reconstruct the harmonic distortion part of the grid voltage, which is later subtracted from the original signal as shown in the scheme of Fig. 2.3. Notice that the difference with respect to the diagram of Fig. 4.1 is simply the introduction of the feedback block UHCM. Hence the UHCM can be seen as plug-in block that can be easily added to the basic scheme U-PLL. This scheme represents an alternative to the harmonic compensation scheme reported in [21].

Based on the model (4.9)-(4.10), the estimator for the kth harmonic component (k ∈ H) can be proposed as follows

$$\dot{\hat{V}}_{\alpha\beta,k} = k\widehat{\omega_0}\mathrm{J}\,\hat{\varphi}_{\alpha\beta,k} + \gamma_k\tilde{V}_{\alpha\beta} \tag{4.15}$$

$$\dot{\hat{\varphi}}_{\alpha\beta,k} = k\widehat{\omega_0}\mathrm{J}\,\hat{V}_{\alpha\beta,k} \tag{4.16}$$

Where γ_k is a positive design parameter used to introduce the required damping;

$\widehat{\omega_0}$ is the estimate of parameter ω_0 to be defined later; and $\tilde{V}_{\alpha\beta} \cong V_{\alpha\beta} - \hat{V}_{\alpha\beta}$, with $\hat{V}_{\alpha\beta}$ representing the estimated voltage .In fact, the estimated voltage signal $\hat{V}_{\alpha\beta}$can be decomposed as follows

$$\hat{V}_{\alpha\beta} = \hat{V}_{\alpha\beta,1} + \hat{V}_{\alpha\beta,h} \quad (4.17)$$

Where $\hat{V}_{\alpha\beta,1}$ represents the estimate of the fundamental component and $\hat{V}_{\alpha\beta,h}$ represents the estimate of the harmonic distortion components of the grid voltage. From (4.15)-(4.16), it is clear that the fundamental component $\hat{V}_{\alpha\beta,1}$is reconstructed according to

$$\dot{\hat{V}}_{\alpha\beta,1} = \widehat{\omega_0} \mathrm{J}\, \hat{\varphi}_{\alpha\beta,1} + \gamma_1 \tilde{V}_{\alpha\beta} \quad (4.18)$$

$$\dot{\hat{\varphi}}_{\alpha\beta,1} = k\widehat{\omega_0} \mathrm{J}\, \hat{V}_{\alpha\beta,1} \quad (4.19)$$

Notice that the estimator (4.18)-(4.19) similar to the U-AQSG in (4.10)-(4.11), except a new equation of $\tilde{V}_{\alpha\beta} \cong V_{\alpha\beta} - \hat{V}_{\alpha\beta}$, which includes the harmonic contents according to (4.17). Hence, this part of the scheme will be referred as UH-AQSG. The harmonic distortion component $\hat{V}_{\alpha\beta,h}$computed in block UHCM is performed as follows [13]. First, each harmonic component is reconstructed according to (4.15)-(4.16) for k ∈{3, 5, ...}. Second, all harmonic components are accumulated in a single signal as follows.

$$\hat{V}_{\alpha\beta,h} = \sum_{K\in\{3,5\ldots\}} \hat{V}_{\alpha\beta,k} \quad (4.20)$$

Reconstruction of signal $\widehat{\omega_0}$ involved in (4.18) and in the UHCM is performed by the following adaptive law

$$\dot{\widehat{\omega}}_0 = \lambda \tilde{V}_{\alpha\beta}^{\ T} \mathrm{J} \hat{\varphi}_{\alpha\beta,1} \quad (4.21)$$

Whereas before, $\lambda > 0$ represents the adaptation gain, and J was defined in (4.2). Notice that (4.21) coincides with the U-FFE described in (4.12) except for the new definition of $\tilde{V}_{\alpha\beta}$.It includes the harmonic contents according to (4.17).Therefore this part of the scheme will be referred as UH-FFE. As before, a scheme is proposed to generate the positive and negative sequences of the fundamental component of the grid voltage (F-PNSG).

$$V^p_{\alpha\beta,1} = \frac{1}{2}(\hat{V}_{\alpha\beta,1} + \hat{\varphi}_{\alpha\beta,1}) \quad (4.22)$$

$$V^n_{\alpha\beta,1} = \frac{1}{2}(\hat{V}_{\alpha\beta,1} - \hat{\varphi}_{\alpha\beta,1}) \quad (4.23)$$

4.2.6 TUNING OF THE UH-PLL ALGORITHM

Some rules for a tuning of control parameters λ and γ_k (k ∈ H) are presented [13]. For this purpose, some simplifications are considered. First, Non distorted case is considered, i.e., no UHCM block is included. Second, it is considered that the system is in balanced operation, that is, ϕαβ~= vαβ. Finally, a linearization process is considered. These simplifications yield a LTI system which coincides with the one studied in [22], where they propose to tune the parameters according to the following expressions.

$$\lambda \cong \sqrt{2}\omega_{BW} \tag{4.24}$$

$$\gamma_1 = \left(\frac{\omega_{BW}}{|V_{\alpha\beta}|}\right)^2 \tag{4.25}$$

Where ω_{BW} is basically the desired bandwidth of the fundamental frequency estimator, which is recommended to be selected in the range $\frac{\omega_0}{5} \leq \omega_{BW} \leq \frac{\omega_0}{2}$. For the rest of the gains γ_k (k ∈ {3, 5, ...}) a first tuning rule can be stated as follows.

The influence of the second order system frequency response, each gain γ_k can be fixed at

$$\gamma_k = \left(\frac{2.2}{T_{sk}}\right), \text{k} \in \{3, 5, ...\} \tag{4.26}$$

Where T_{sk} is the response time of each harmonic component (evaluated between 10%-90% of a step response of the amplitude of the corresponding sinusoidal perturbation) .

4.3.1 Response of UH PLL During Unbalanced Grid Voltages

The following parameters have been selected λ = 300 and γ1= 1.5, which correspond approximately for a bandwidth of ω_{BW} =150 rad/s (24 Hz). It is assumed that the grid voltage signal contains 3rd and 5th harmonics, and thus the UHCM contains UHOs tuned at these harmonics. The grid voltage has a nominal frequency of ω_0=314.16 rad/s(50 Hz), and an approximate amplitude of |vαβ| = 100 V.

The following cases have been considered for the utility voltage:

(i) **Unbalanced condition:**. The voltage source includes both a positive and a negative sequence components. The positive sequence has 100 V of amplitude at 314.16 rad/s (50 Hz) and zero phase shift. For the negative sequence an amplitude of 10V approximately and zero phase shift are considered.

(ii) **Harmonic distortion:** Harmonics 3rd and 5th are added to the previous unbalanced signal to create a periodic distortion. Both harmonics have also a negative sequence component to allow unbalance in harmonics as well. Both positive and negative sequences of these harmonics have 10 V of amplitude and zero phase shift.

Figure 4.2 shows the transient response obtained with the pro-posed UH-PLL when the utility voltage goes from a balanced to an unbalanced operation condition at time t = 1 s Fig. 4.2 (a). From Fig 4.2 (b) Notice that, after a relatively short transient the signal returns to their desired value of 100π. From Fig.4.2 (c) The phase angle which is the time integration of angular frequency is perfectly triangular as there were only small transients in the angular frequency. From Fig.4.2 (d) It can be concluded that the estimated positive-sequence voltages have an almost imperceptible variation.

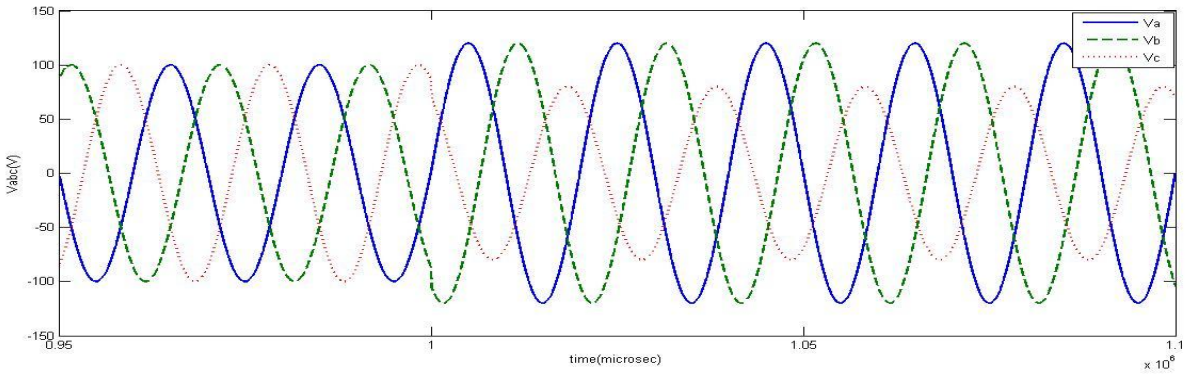

Fig.4.2(a)

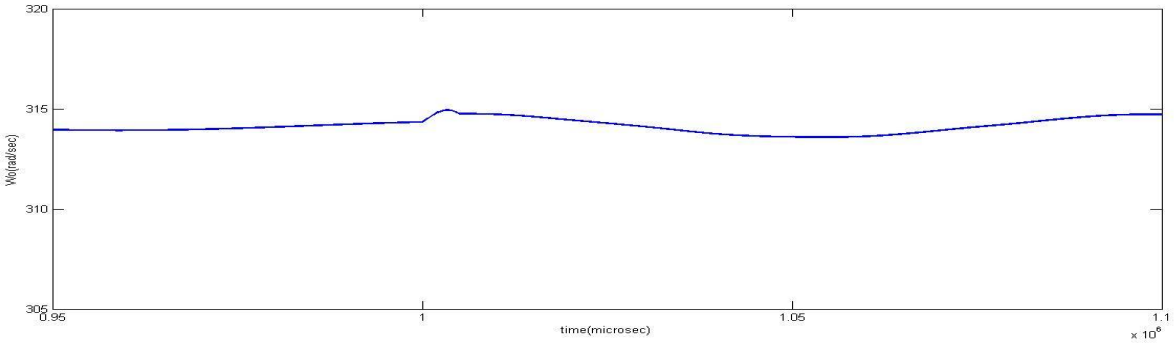

Fig.4.2(b)

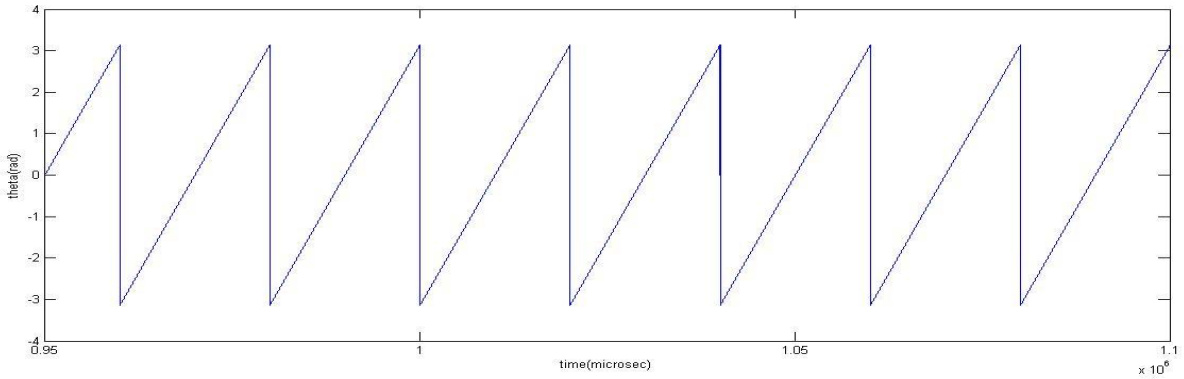

Fig.4.2(c)

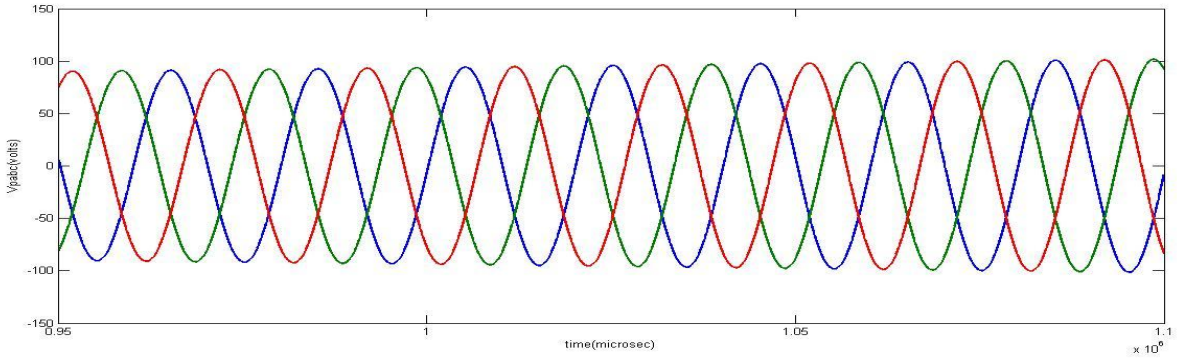

Fig.4.2(d)

Fig. 4.2 a) Unbalanced Supply Voltage ; b) ω_0 estimate (rad/sec), c) θ_0 estimate (rad), d) estimated positive sequence voltage in three-phase coordinates.

4.3.2 Response of UHPLL During Distorted Harmonic Grid Condition

Figure 4.3 shows the transient response of the proposed UH-PLL when harmonic distortion is added to the already unbalanced grid voltage at t = 1.8s Fig 4.3 (a). Notice that, after a relatively short transient, all signals return to their desired values. In particular, notice that the estimated frequency is also maintained in its reference fixed to 314.14 rad/s after a small transient, without further fluctuations Fig 4.3(b). From Fig 4.3 (c) The phase angle which is the time integration of angular frequency is perfectly triangular as there were only small transients in the angular frequency. Moreover, notice that the estimated positive-sequence voltages has an almost imperceptible transient.

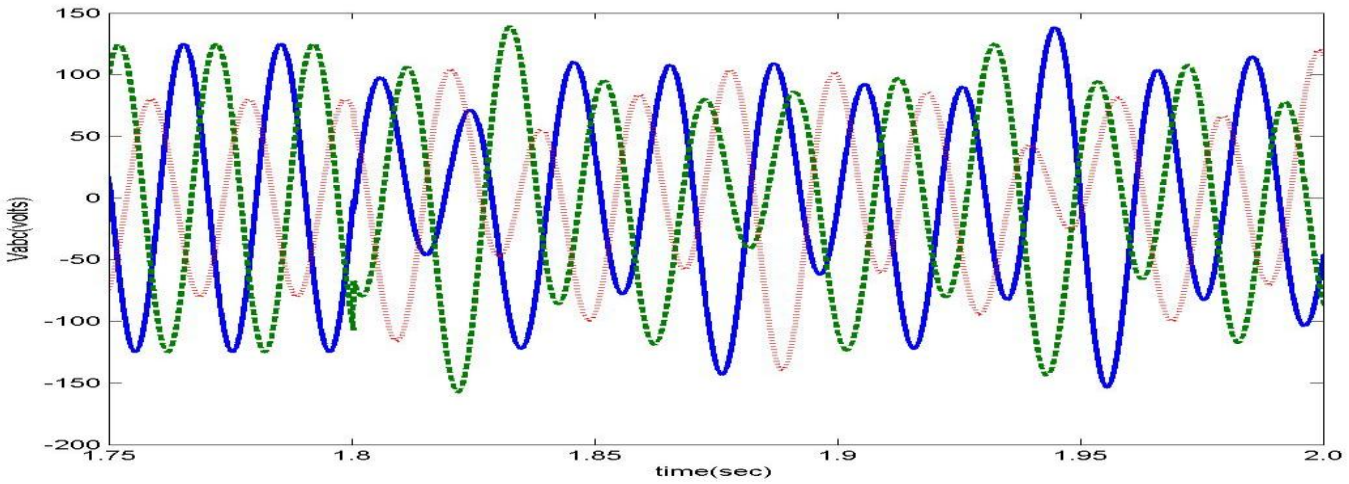

Fig.4.3 (a)

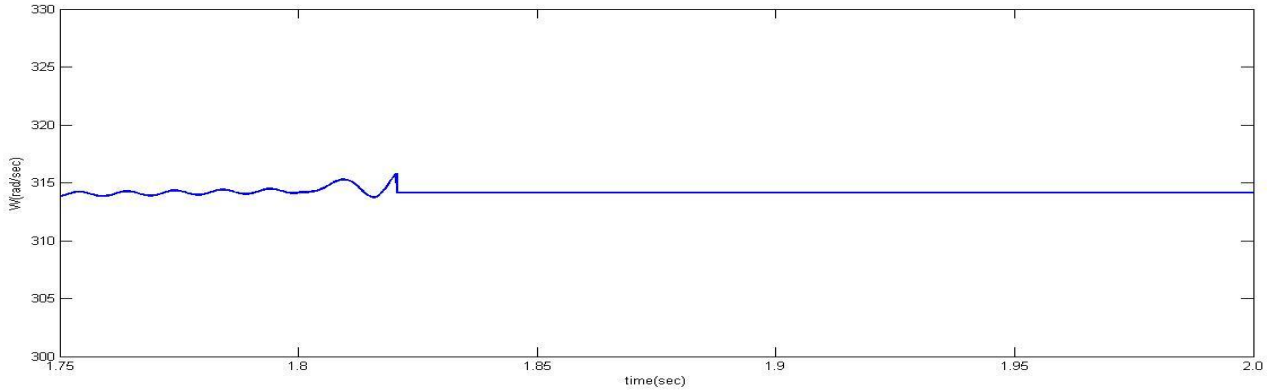

Fig.4.3 (b)

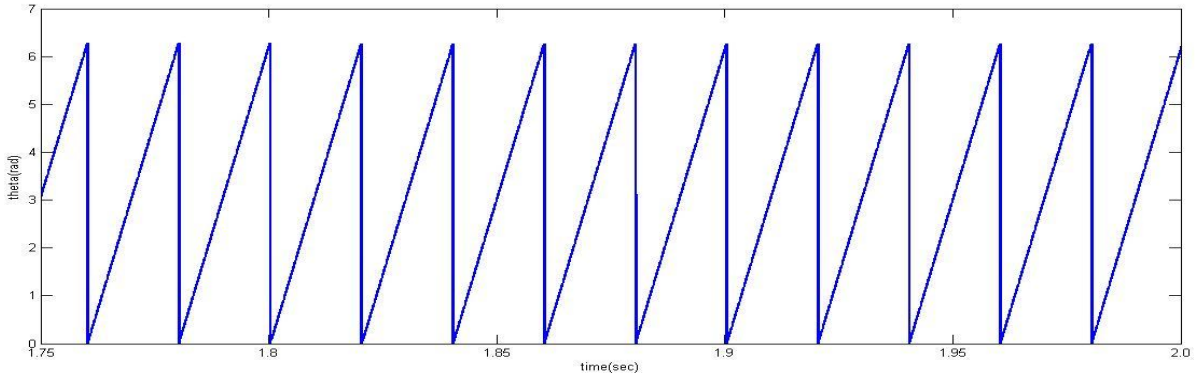

Fig.4.3 (c)

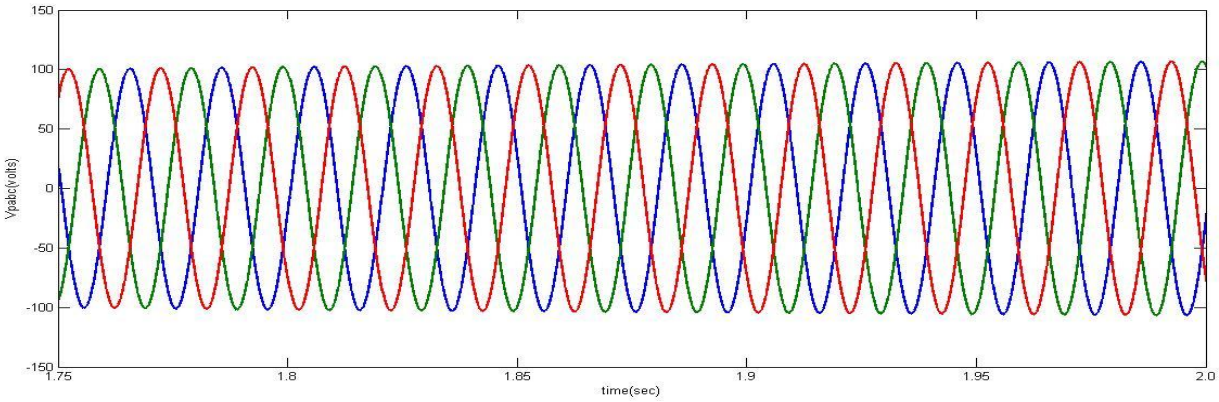

Fig.4.3 (d)

Fig. 4.3 a) Unbalanced Supply Voltage ; b) ω_0 estimate (rad/sec), c) θ_0 estimate (rad), d) estimated positive-sequence voltage in three-phase coordinates.

4.3 CONCLUSION:

This chapter presented a PLL method based on the detection of the fundamental frequency approach. It comprised of estimator for the positive-sequence component of a three-phase signal and an adaptive law to reconstruct fundamental frequency. The design was based on description of an unbalanced and distorted signal expressed in fixed frame coordinates. The method was thus referred as UH-PLL. It was observed that in spite of an unbalanced and distorted reference signal the UH-PLL was able to deliver pure balanced sinusoidal signal represented by the positive sequence component of the reference signal, plus a ripple free fundamental frequency estimated signal. As the UH-PLL includes an explicit mechanism to compensate harmonics, it reduced considerably the effect of disturbances without compromising the speed of response of the overall scheme. In cases of low distortion, this mechanism can be easily disconnected and rely on the selective nature of a basic method, which can be enhanced at the expenses of reducing the speed of response of the overall scheme.

CHAPTER 5

Conclusions

5.1 CONCLUSION:

The various grid synchronization algorithms were analyzed in this thesis and the following conclusions are drawn.

A. A Synchronous Reference Frame (SRF) PLL can be used for 3-phase balanced signals. But it cannot be used for unbalanced utility conditions as the detected phase angle contains 2^{nd} harmonic oscillations.

B. Double SRF PLL solves the above problem by decomposing the input voltage vectors into their positive and negative sequence components. This PLL detects the phase angle separately for each of the two components. The response of this PLL has slight oscillations which makes the response sluggish in nature.

C. As the UH-PLL includes an explicit mechanism to compensate harmonics, it reduced considerably the effect of disturbances without compromising the speed of response of the overall scheme when compared to other PLL schemes .

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